

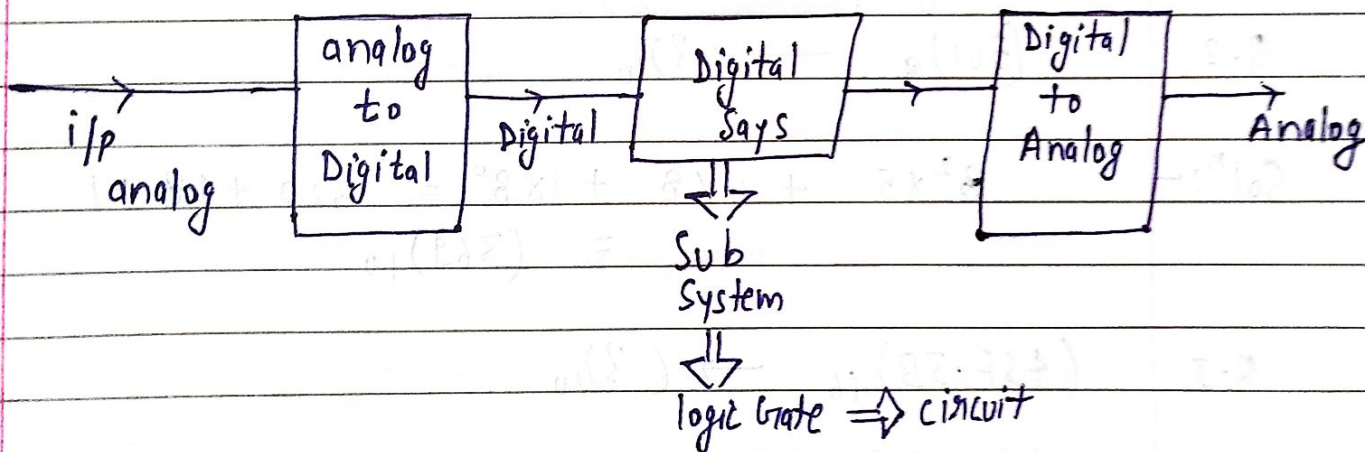
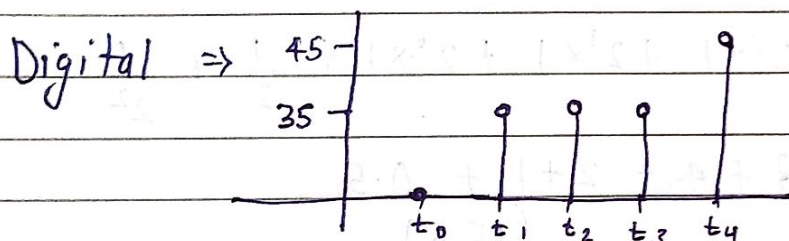
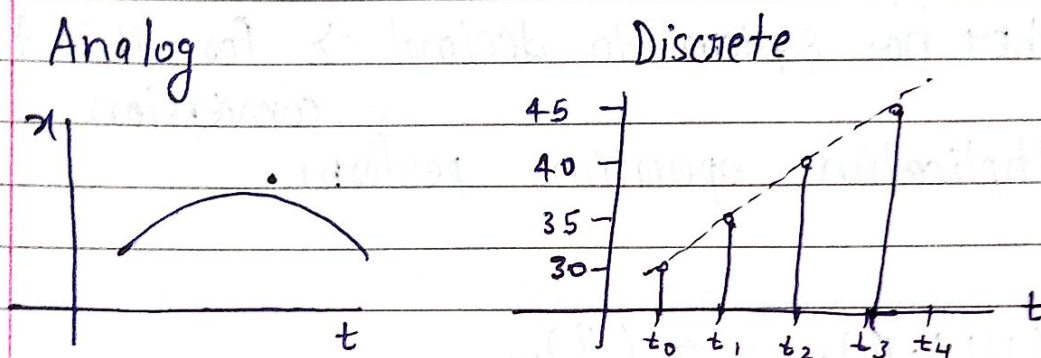
Unit - 1

Fundamental Concept

POPU

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Signal:- Signal is the function that represents the variation of any physical quantity w.r.t. any parameter.



Number System $\Rightarrow$ defines set of values used to represent quantity

- (i) Binary System $\Rightarrow$ 0, 1 2 no.
- (ii) Octal System $\Rightarrow$ 0 to 7 8 no.
- (iii) Decimal System $\Rightarrow$ 0 to 9 10 no.
- (iv) Hexadecimal System $\Rightarrow$ 0 to 9, A to F 16 no.

(i) ~~Q~~ Decimal to other no. system $\Rightarrow$ In this conversion to convert the decimal division operation is performed successfully on the question.

(ii) Other no. system to decimal $\Rightarrow$ For this type of conversion multiplication operation perform.

Eg-1 $(1111.10)_2 \rightarrow (?)_{10}$

Ans - $2^3 \times 1 + 2^2 \times 1 + 2^1 \times 1 + 2^0 \times 1 + \frac{1}{2} + \frac{0}{2^2}$
 $8 + 4 + 2 + 1 + 0.5$
 $(15.5)_{10}$

Q.2 $(561)_8 \rightarrow (?)_{10}$

Solⁿ:- $8^2 \times 5 + 6 \times 8 + 1 \times 8^0 = 320 + 48 + 1$
 $= (369)_{10}$

Q.3 $(43F.3B)_{16} \rightarrow (?)_{10}$

Solⁿ:- $4 \times 16^2 + 3 \times 16 + 15 \times 16^0 + \frac{3}{16} + \frac{11}{16^2}$
 $256 \times 4 + 16 \times 3 + 15 \times 1 + 0.18 + 0.05$
 $(1087.23)_{10}$

Q.4 $(135.23)_{10} \rightarrow (?)_2$

Solⁿ:-

2	135	1
2	67	1
2	33	1
2	16	0
2	8	0
2	4	0
2	2	0
1		

10000111

$$0.23 \times 2 = 0.46 = 0$$

$$0.46 \times 2 = 0.92 = 0$$

$$0.92 \times 2 = 1.84 = 1$$

$$(10000111.001)_2$$

Q.5 $(4372.1134)_{10} \rightarrow (?)_{16}$

Solⁿ:-

16	4372	4
16	273	1
16	17	1
1		

(1114)

$$0.1134 \times 16 = 1.814 = 1$$

$$0.814 \times 16 = 13.024 = D$$

$$(1114.D)_{16}$$

Q.6 $(E7.18)_{16} \rightarrow (?)_2$

Solⁿ

Step-I $(E7.18)_{16} \rightarrow (?)_{10}$

$$14 \times 16 + 7 \times 16^0 + \frac{1}{16} + \frac{8}{256}$$

$$= 224 + 7 + 0.06 + 0.03$$

$$(231.09)_{10}$$

Step-II $(231.09)_{10} \rightarrow (?)_2$

2	231	1
2	115	1
2	57	1
2	28	0
2	14	0
2	7	1
2	3	1
	1	

11100111

$$0.09 \times 2 = 0.18$$

$$0.18 \times 2 = 0.36$$

$$0.36 \times 2 = 0.72$$

$(11100111.000)_2$

H.W.

Q.7

Soln:-

$(DE \cdot AB)_{16} = (?)_8$
Step-I

$(DE \cdot AB)_{16} \rightarrow (?)_{10}$

$$16^1 \times 13 + 16^0 \times 14 + \frac{10}{16} + \frac{11}{256}$$

$$208 + 14 + 0.625 + 0.042$$

$$222 + 0.667$$

$$(222.667)_{10}$$

Step-II $(222.667)_{10} \rightarrow (?)_8$

8	222	6
8	27	3
	3	

336

$$0.667 \times 8 = 5.336 = 5$$

$$0.336 \times 8 = 2.688 = 2$$

$$0.688 \times 8 = 5.504 = 5$$

$$(336.596)_8$$

Q.8
Solⁿ

$$(87E)_{16} = (?)_5$$

$$(87E)_{16} \rightarrow (?)_{10}$$

$$8 \times 16^2 + 7 \times 16 + 14 \times 16^0$$

$$8 \times 256 + 112 + 14 = 2048 + 128$$

$$(2174)_{10}$$

$$(2175)_{10} \longrightarrow (?)_5$$

5	2174	4
5	434	4
5	86	2
5	17	2
	3	

$$(\cancel{32200})_5$$

Ans

$$(32144)_5$$

Q.9
Solⁿ

$$(1011.11)_2 \rightarrow (?)_7$$

$$(1011.11)_2 \rightarrow (?)_{10}$$

$$2^3 \times 1 + 2^2 \times 0 + 2 \times 1 + 2^0 \times 1 + \frac{1}{2} + \frac{1}{4}$$

$$8 + 0 + 2 + 1 + 0.5 + 0.25$$

$$(11.75)_{10}$$

$$(11.75)_{10} \rightarrow (?)_7$$

7	11	4
	1	

$$(14)$$

$$0.75 \times 7 = 5.25 = 5$$

$$0.25 \times 7 = 1.75 = 1$$

$$(14.51)_7$$

Q.10
Soln

$$(179.52)_{10} = (?)_2 = (?)_8 = (?)_{16}$$

$$(a) (179.52)_{10} = (?)_2$$

2	179	1
2	89	1
2	44	0
2	22	0
2	11	1
2	5	1
2	2	0
	1	

$$0.52 \times 2 = 1.04 = 1$$

$$0.04 \times 2 = 0.08 = 0$$

$$0.08 \times 2 = 0.16 = 0$$

$$(10110011.10)_2$$

$$(b)$$

8	179	3
8	22	6
	2	

$$0.52 \times 8 = 4.16 = 4$$

$$0.16 \times 8 = 1.28 = 1$$

$$(263.44)_8$$

$$(c)$$

16	179	3
	11	

B3

$$0.52 \times 16 = 8.32 = 8$$

$$0.32 \times 16 = 5.12 = 5$$

$$(B3.85)_{16}$$

Addition, subtraction, multiplication: -

$$0 + 0 = 0$$

$$0 + 1 = 1$$

$$1 + 0 = 1$$

$$1 + 1 = 10$$

↓
Carry

$$\begin{array}{r} \text{Q.} \quad 1010 \\ + 1111 \\ \hline 11001 \end{array}$$

$$\begin{array}{r} \text{Q.} \quad 1001 \\ + 0111 \\ \hline 10000 \end{array}$$

$$\begin{array}{r} \text{Q.} \quad 1001 \\ - 0111 \\ \hline 0010 \end{array}$$

$$\begin{array}{r} \text{Q.} \quad 1010 \\ \times 1101 \\ \hline 1010 \\ 0000 \\ 1010 \\ 1001 \\ \hline 1000010 \end{array}$$

Division: -

$$\begin{array}{r} \text{Q.} \quad 101 \overline{) 11001} (10 \\ \underline{101} \\ 00101 \\ \underline{101} \\ 000 \end{array}$$

$$\begin{array}{l} (162)_8 + (557)_8 \\ \hline (721)_8 \checkmark \\ (36)_8 + (636)_8 \\ \hline (774)_8 \end{array}$$

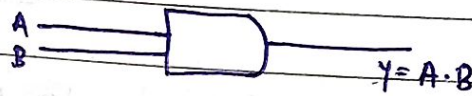
$$\begin{array}{r} \text{Q.} \quad 1100 \overline{) 11101} (10.01 \\ \underline{1100} \\ 0010100 \\ \underline{1100} \\ 10000 \\ \underline{10000} \\ 0000 \end{array}$$

$$\begin{array}{r} 362 \\ 1921 \end{array}$$

Logic Gates: - (7)

Basic Logic Gates	Universal	Combination
→ AND	→ NAND	→ XOR
→ NOT	→ NOR	→ XNOR
→ OR		

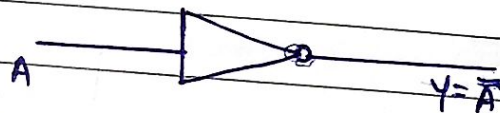
(i) AND ⇒



i/p		o/p
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

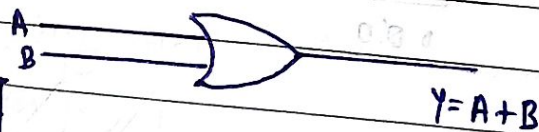


(ii) NOT

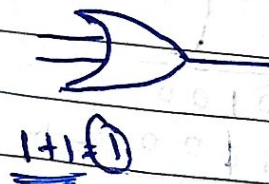


i/p (A)	o/p ($\bar{A}$)
0	1
1	0

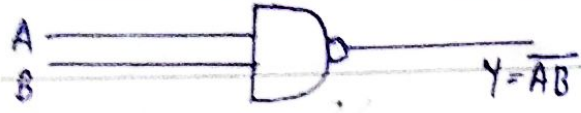
(iii) OR



i/p		o/p
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



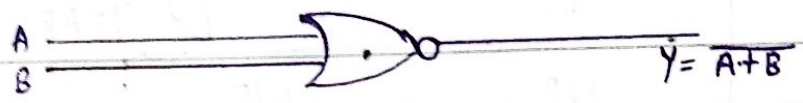
(iv) NAND



I/P		O/P
A	B	$Y = \overline{AB}$
0	0	1
0	1	1
1	0	1
1	1	0

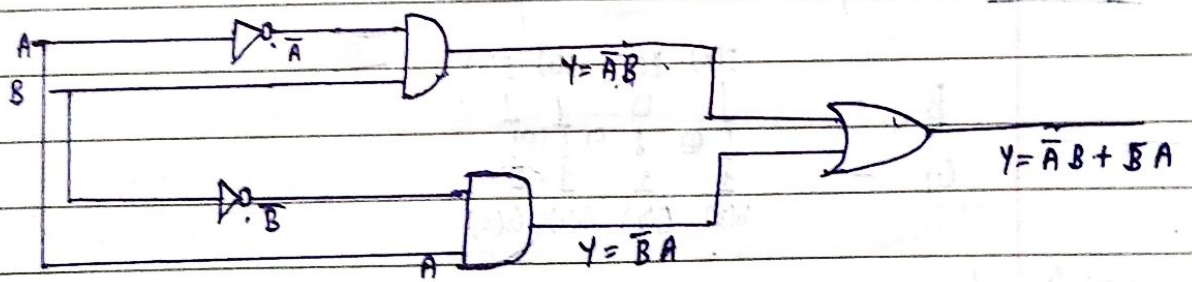
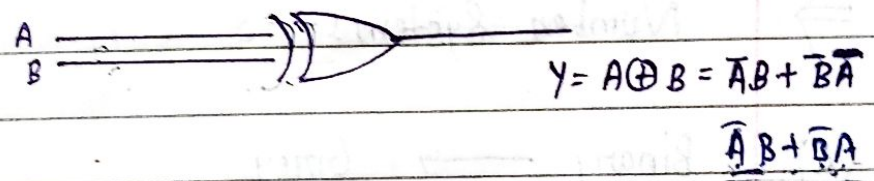
$\overline{0} = 1$
 $\overline{0} = 1$
 $\overline{0} = 1$
 $\overline{1} = 0$

(v) NOR



I/P		O/P
A	B	$Y = \overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0

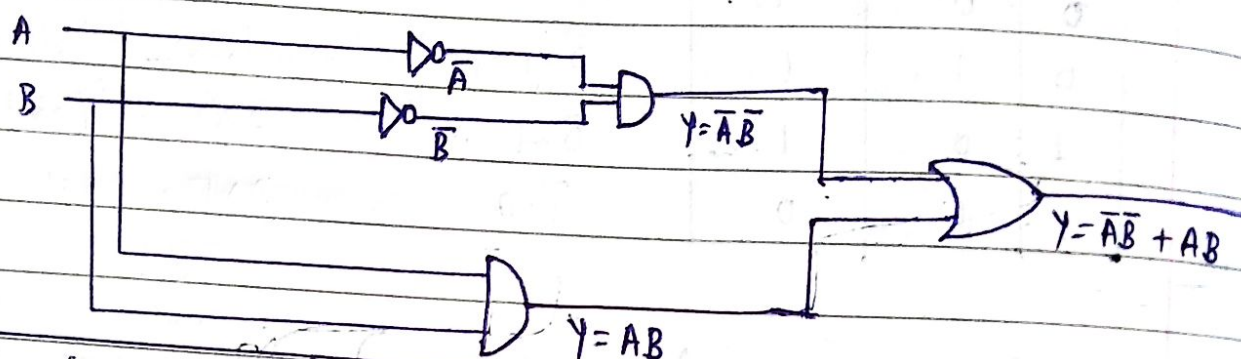
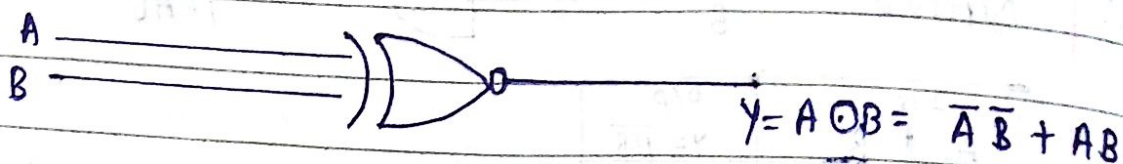
(vi) XOR



I/P		O/P
A	B	$Y = A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

(vii)

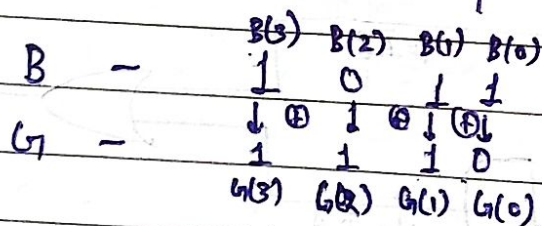
XNOR :-



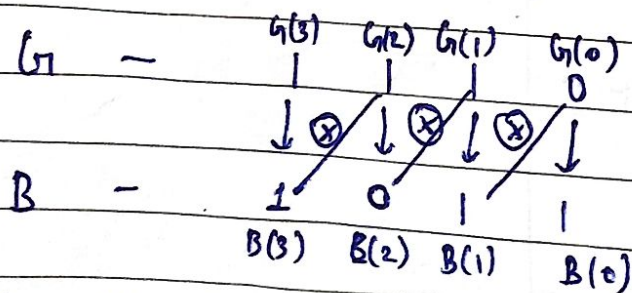
i/p		o/p $Y = A \odot B$
A	B	
0	0	1
0	1	0
1	0	0
1	1	1

⇒ Number System :-

(A) Binary → Grey



(B) Grey → Binary



Theoretical representation ⇒

(A)

B to G

(i) $G(3) \rightarrow B(3)$

(ii) $G(2) \rightarrow B(3) \oplus B(2)$

(iii) $G(1) \rightarrow B(2) \oplus B(1)$ ✓

(iv) $G(0) \rightarrow B(1) \oplus B(0)$

(B)

G to B

(i) $B(3) \rightarrow G(3)$

(ii) $B(2) \rightarrow B(3) \oplus G(2)$

(iii) $B(1) \rightarrow B(2) \oplus G(1)$

(iv) $B(0) \rightarrow B(1) \oplus G(0)$

Compliments $\Rightarrow$

Binary - 1's compliments $\Rightarrow$ $1011 \rightarrow 0100 - 1's$

2's compliments $\Rightarrow$

Q. 1011

Ans - 0100

+ 1

0101 — 2's of 1011

Decimal 9's compliments $\Rightarrow$

$n = \text{no. of digits in given no.}$
 $N = \text{given no.}$

$R^n - N - 1 = 10^n - N - 1$

$n \text{ times } 9 - N$

$99 - 89 = 10$

$(89)_{10} = 10^2 - 89 - 1 = 10$

10's compliments $\Rightarrow$

$R^n - N = 10^n - N$

$(89)_{10} = 10^2 - 89 = 11$

- Q. (i) 748
 (ii) 649
 (iii) 891

Ans - (i) 10's complement of 748 is
 $(10)^3 - 748$
 $= 1000 - 748$
 $= 252$

9's complement of 748 is
 $(10)^3 - 748 - 1$
 $= 251$

(ii) $(10)^3 - 649$
 $= 1000 - 649$
 $= 351$

$(10)^3 - 649 - 1$
 $= 1000 - 650$
 $= 350$

(iii) $(10)^3 - 891$
 $= 109$

$(10)^3 - 891 - 1$
 $= 108$

Q. 1 Subtract $(1010)_2$ from $(1111)_2$ using 1's

Ans -

$$\begin{array}{r} 1111 \\ - 1010 \\ \hline 0101 \end{array}$$

Direct method

Using 1's

$$\begin{array}{r} 1111 \\ + 0101 \quad - 1's \text{ of } (1010)_2 \\ \hline 10100 \\ \downarrow \text{Carry} \\ + \quad \quad \quad 1 \rightarrow \text{Add carry 1} \\ \hline 0101 \end{array}$$

Q. 2 Subtract $(1010)_2$ from $(1111)_2$ using 2's

$$\begin{array}{r} 1111 \\ 0101 \\ \hline \end{array}$$

$$\begin{array}{r} 1010 \\ \downarrow \\ 0101 \\ + 1 \\ \hline 0110 \rightarrow 2's \end{array}$$

$$\begin{array}{r} 1111 \\ + 0110 \text{ --- } 2's \text{ of } (1010)_2 \\ \hline 10101 \\ \text{sign bit} \leftarrow \\ \hline 0110 \\ \hline 0110 \end{array}$$

$\left. \begin{array}{l} 1 \rightarrow +ve \\ 0 \rightarrow -ve \end{array} \right\} \begin{array}{l} \text{carry} \\ \text{carry} \end{array}$

Ans - 0101

Q. 3 $(1000)_2 - (1010)_2$ using 2's

Ans -

$$\begin{array}{r} 1010 \\ \downarrow \\ 0101 \\ + 1 \\ \hline 0110 \text{ --- } 2's \text{ of } (1010)_2 \end{array}$$

Normal

$$\begin{array}{r} 1000 \\ - 1010 \\ \hline -0010 \end{array}$$

$$\begin{array}{r} 1000 \\ + 0110 \\ \hline 1110 \end{array}$$

No carry obtained,
Thus the value is negative.

$$\begin{array}{r} -1110 \\ \downarrow \end{array}$$

$$\begin{array}{r} -0001 \rightarrow 2's \text{ of } (-1110)_2 \\ + 1 \\ \hline -0010 \end{array}$$

Q. $649 - 387$ using 10's

Ans-

$$(387)_{10}$$

$$10^3 - 387 = 613$$

$$\begin{array}{r} 649 \\ 613 \\ \hline 1262 \end{array}$$

10's $\rightarrow$ Sign carry
9's $\rightarrow$ carry

$\rightarrow$ 10 is sign +ve

$$(262)_{10}$$

Q. $649 - 387$ using 9's

$$(387)_{10}$$

$$10^3 - 387 - 1 = 612$$

$$\begin{array}{r} 649 \\ 612 \\ \hline 1261 \\ \rightarrow +1 \rightarrow \text{add carry} \\ \hline 262 \end{array}$$

Q.1 Subtract $(1010)_2$ from $(1000)_2$ using 1's

Q.2 Subtract $(1011)_2$ from $(1110)_2$ using 2's

Q.3 Subtract using 9's

(a) $39 - 23$

(b) $49 - 84$

(c) $891 - 786$

Q4 Subtract using 10's

(a) $786 - 427$

(b) $473 - 438$

Ans ①

$$\begin{array}{r} 1000 \\ + 0101 \rightarrow \text{1's of } (1010)_2 \\ \hline 1101 \end{array}$$

No carry will be generated negative sign.

$$\begin{array}{r} -1101 \\ \downarrow \\ \hline 0010 \rightarrow \text{1's of } (-1101)_2 \end{array}$$

Ans ②

$$\begin{array}{r} = (1110)_2 \\ 1011 \\ \downarrow \\ 0100 \\ + 1 \\ \hline 0101 \rightarrow \text{2's of } (1011)_2 \end{array}$$

$$\begin{array}{r} 1110 \\ + 0101 \\ \hline 10011 \\ \swarrow \text{true} \\ \hline \cancel{0} \cancel{0} \cancel{0} \end{array} \quad \text{Ans} \Rightarrow 0011$$

Ans ③

Using 9's

$39 - 23$

$(23)_{10}$

$10^2 - 23 - 1 = 76$

$$\begin{array}{r} 110 \\ 101 \\ - 101 \\ \hline \end{array}$$

$$\begin{array}{r}
 28 \quad 39 \\
 \underline{76} \\
 115 \\
 \leftarrow +1 \text{ -- carry} \\
 \underline{116}
 \end{array}$$

$$A_y \Rightarrow 16$$

(b)

$$\begin{array}{r}
 49 - 84 \\
 (84)_{10} \\
 10^2 - 84 - 1 \\
 99 - 84 = 15
 \end{array}$$

9's compliment is taken by

Now

$$\begin{array}{r}
 49 \\
 + 15 \\
 \hline
 64
 \end{array}$$

No carry will be obtained
 so sign will be negative
 Difference

then

$$\begin{array}{r}
 10^2 - 64 - 1 \\
 = 99 - 64 \\
 = 35
 \end{array}$$

$$A_y \rightarrow -35$$

(c)

$$\begin{array}{r}
 891 - 786 \\
 9's \text{ compliment of } (786)_{10} \\
 = 1000 - 786 - 1 \\
 = 213
 \end{array}$$

then

$$\begin{array}{r}
 891 \\
 \underline{213} \\
 1104
 \end{array}$$

Carry

$$\begin{array}{r} 104 \\ + 1 \\ \hline 105 \end{array}$$

$$105 - 105$$

Ans ④ Using 10's compliments: —

(9) $786 - 427$

10's compliment is taken by
 $103 - 427$

$$1000 - 427$$

$$= (573)_{10}$$

then

$$786$$

$$573$$

$$\begin{array}{r} \text{Sign} \leftarrow \text{①} 573 \\ +ve \end{array}$$

then

$$\boxed{\text{Ans} \Rightarrow 359}$$

(b) $473 - 438$

10's compliment of $(438)_{10}$ is taken by

$$103 - 438 = (562)_{10}$$

then

$$473$$

$$562$$

$$\begin{array}{r} \text{Sign} \leftarrow \text{①} 035 \\ +ve \end{array}$$

then

$$\boxed{\text{Ans} \Rightarrow 35}$$

Q.
Ans -

$(1010)_2 - (1000)_2$ using 1's

$$\begin{array}{r}
 1010 \\
 + 0111 \\
 \hline
 10001 \\
 \text{Carry} \swarrow + 1 \rightarrow \text{Add carry} \\
 \hline
 0010
 \end{array}$$

Q.
Ans -

$(1111)_2$ from $(1000)_2$ using 2's

$$\begin{array}{r}
 1111 \\
 \text{1000} \rightarrow \text{1's complement} \\
 + 1 \\
 \hline
 0001 \rightarrow \text{2's complement}
 \end{array}$$

$$\begin{array}{r}
 1000 \\
 0001 \\
 \hline
 1000 \rightarrow \text{+ve}
 \end{array}$$

$$\begin{array}{r}
 1000 \\
 + 0001 \\
 \hline
 1001
 \end{array}$$

No carry will be generated Thus the diff. will be negative.

$$\begin{array}{r}
 0110 \\
 + 1 \\
 \hline
 0111
 \end{array}$$

Ans

BCD (Binary coded Decimal) $\Rightarrow$ It is fast & efficient system to convert the decimal no. into binary no.

$$\begin{array}{r}
 1001 \\
 + 0100 \\
 \hline
 1101
 \end{array}$$

$\rightarrow$ Invalid BCD

$\left\{ \begin{array}{l} +4 \\ 13 \end{array} \right\}$

Ex 21

$$\begin{array}{r}
 1101 \\
 + 0110 \\
 \hline
 00010011 \\
 \hline
 1 \quad 3
 \end{array}$$

Invalid BCD - Add 6

Q. BCD addition

$$\begin{array}{r}
 1000 \\
 + 0111 \\
 \hline
 1111 \\
 + 0110 \\
 \hline
 00010101 \\
 \hline
 1 \quad 5
 \end{array}$$

Invalid BCD

Q. 19 + 24 by using BCD

$$\begin{array}{r}
 00011001 \\
 + 00100100 \\
 \hline
 00111101 \\
 \downarrow \quad \downarrow \\
 3 \quad 13
 \end{array}$$

Right group is invalid BCD

00111101 - invalid BCD

$$\begin{array}{r}
 001110 \\
 + 01000011 \\
 \hline
 01001111 \\
 \downarrow \\
 4 \quad 3
 \end{array}$$

- Add

$$\begin{array}{r}
 1101 \\
 - 1000 \\
 \hline
 00101 \\
 \hline
 1001 \\
 - 1100 \\
 \hline
 00101 \\
 \hline
 00101
 \end{array}$$

Q. 835 → 10000110101

274 + 001001110100

$$\begin{array}{r}
 10000110101 \\
 + 001001110100 \\
 \hline
 101010101001 \\
 \hline
 10 \quad 10 \quad 9
 \end{array}$$

Invalid Left side two groups BCD

$$\begin{array}{r}
 1010 \quad 1010 \quad 1001 \\
 0110 \quad 0110 \\
 \hline
 0001 \quad 0001 \quad 0000 \quad 1001 \\
 \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \\
 1 \quad 1 \quad 0 \quad 1
 \end{array}$$

— Add 6 in both group

BCD Subtract $\Rightarrow$

(i) $(374)_{10} - (251)_{10}$
 Soln:-

$$\begin{array}{r}
 00110110100 \quad \text{--- } (374)_{10} \\
 - 001001010001 \quad \text{--- } (251)_{10} \\
 \hline
 000100100011 \\
 \textcircled{1} \quad \textcircled{2} \quad \textcircled{3}
 \end{array}$$

(ii) $(546)_{10} - (429)_{10}$

$$\begin{array}{r}
 010101000110 \quad \text{--- } (546)_{10} \\
 - 010000101001 \quad \text{--- } (429)_{10} \\
 \hline
 000100011101 \quad \leftarrow \text{first Right Group invalid BCD} \\
 \textcircled{4} \quad \downarrow - 0110 \quad \text{--- Subtract 6} \\
 \hline
 000100\textcircled{1}10111 \\
 \textcircled{0} \quad \textcircled{1} \quad \textcircled{7}
 \end{array}$$

(iii) $(52532)_{10} - (3257)_{10}$

$$\begin{array}{r}
 52532 \\
 - 3257 \\
 \hline
 49275
 \end{array}$$

$$\begin{array}{r}
 010100100100110010 \quad \text{--- } (52532)_{10} \\
 - 0011001001010111 \quad \text{--- } (3257)_{10} \\
 \hline
 01001111001011011011 \quad \text{--- From Right groups 1, 2 & 4 invalid BCD} \\
 - 0110 \quad 0110 \quad 0110 \\
 \hline
 0100100100101110101 \\
 4 \quad 9 \quad 2 \quad 7 \quad 5
 \end{array}$$

Q. (23)_x + (12)₈ = (18)₁₆
 Ans - $2 \times x + 3 \times x^0 + 1 \times 8 + 2 \times 8^0 = 1 \times 16 + 1 \times 16^0$
 $2x + 3 + 8 + 2 = 16 + 1$
 $2x + 13 = 17$
 $2x = 17 - 13$
 $2x = 4$
 $x = \frac{4}{2}$
 $x = 2$

$x = 7$

Q. (110)_x + (15)_x = (23)_x
 $1 \times x^2 + 1 \times x + 0 \times x^0 + 1 \times x + 5 \times x^0 = 2 \times x + 3 \times x^0$
 $x^2 + x + x + 5 = 2x + 3$
 $x^2 + 2x + 5 = 2x + 3$
 $x^2 = -2$
 $x = \pm \sqrt{2}i$

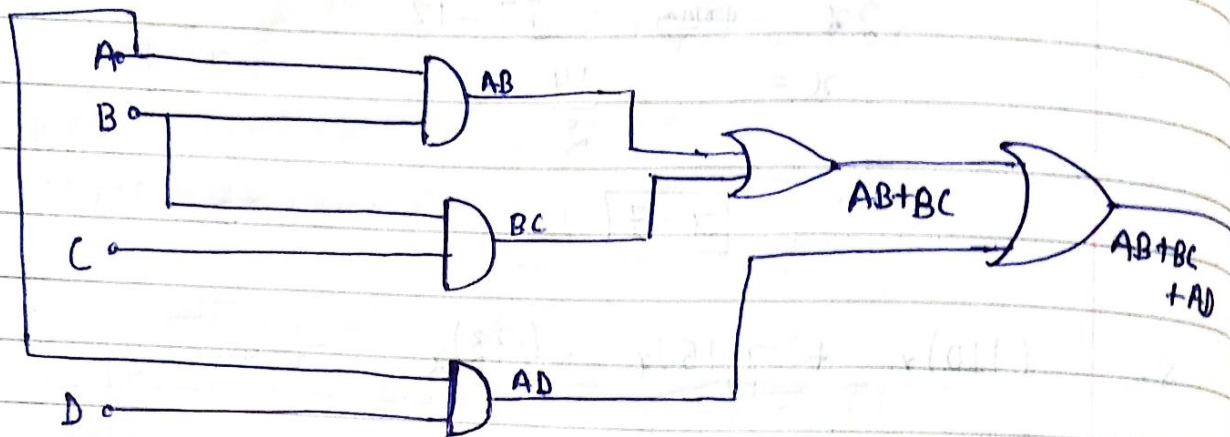
Q. (193)_x = (623)₈
 $x^2 + 9x + 3 = 6 \times 64 + 2 \times 8 + 3 \times 1$
 $x^2 + 9x + 3 = 384 + 16 + 3$
 $x^2 + 9x + 3 = 403$
 $x^2 + 9x - 400 = 0$
 $x = \frac{-9 \pm \sqrt{81 + 1600}}{2}$
 $x = \frac{-9 \pm \sqrt{1681}}{2} = \frac{-9 \pm 41}{2} = 16$

Q. (23)_x + (12)_x = (101)_x
 $2x + 3 + x + 2 = x^2 + 1$
 $x^2 - 3x - 4 = 0$
 $x^2 - 4x + x - 4 = 0 \Rightarrow x(x-4) + 1(x-4)$
 $x = \frac{3 \pm \sqrt{9 + 12}}{2} = \frac{3 \pm \sqrt{21}}{2}$
 $x = 4$

implement of Bullean expression from Logic gate

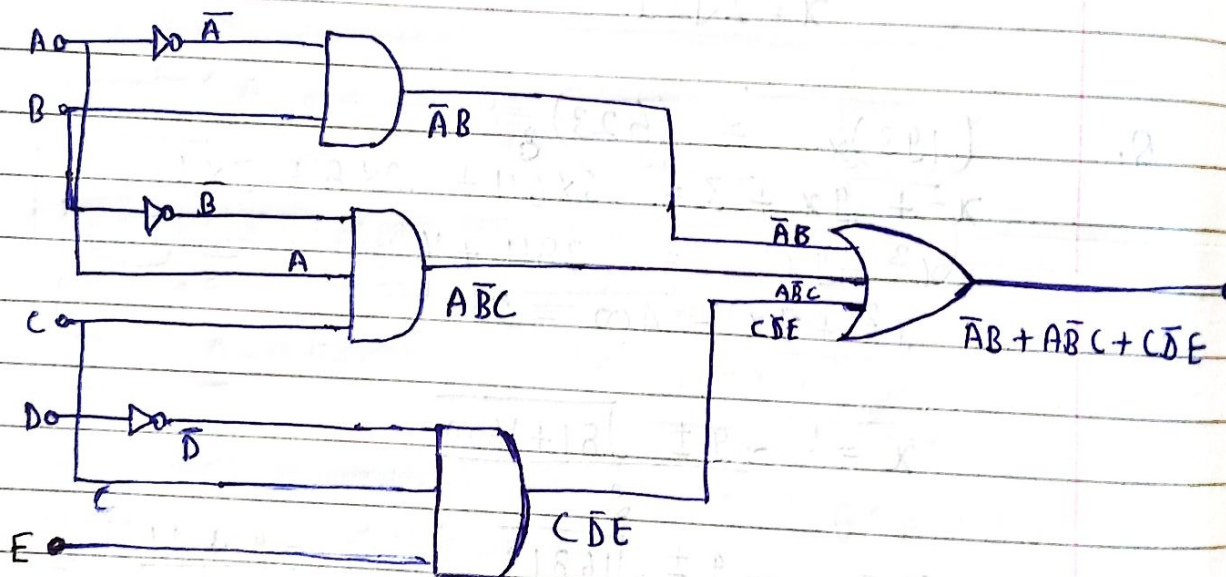
Q. $AB + BC + AD$

A₁ -



Q. $\bar{A}B + A\bar{B}C + C\bar{D}E$

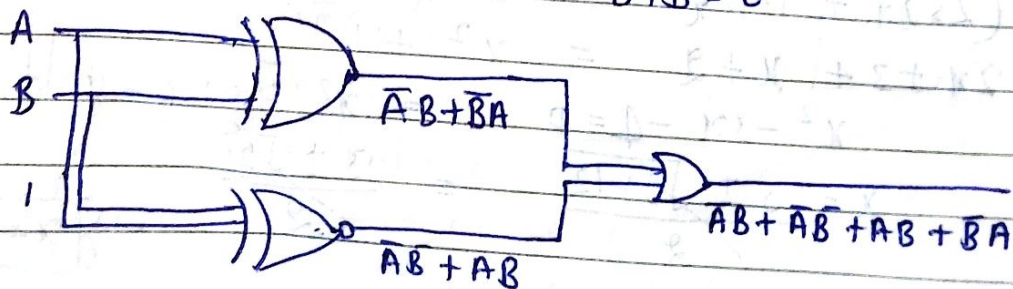
A₁ -



Q. $\bar{A}B + AB + A\bar{B} + \bar{A}\bar{B}$

A₁ -

$$\bar{B}(A + \bar{A}) + \bar{B}(A + \bar{A}) = B + \bar{B} = 1$$

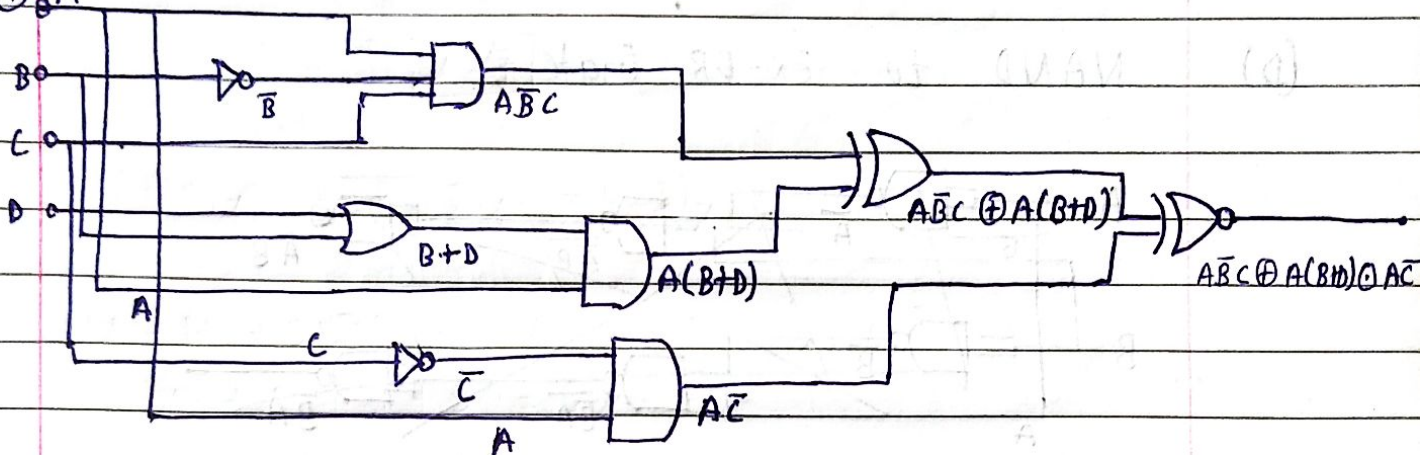


Q.1 $\overline{A}BC \oplus A(B+D) \odot A\overline{C}$

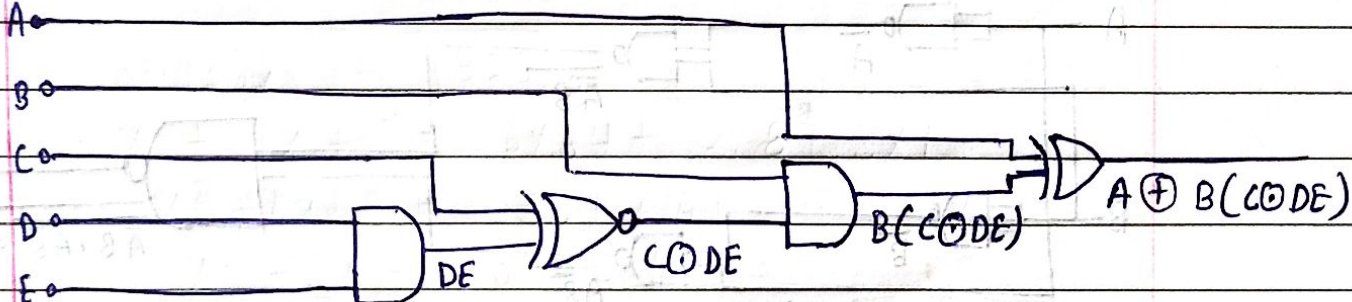
Q.2 $A \oplus B(C \odot DE)$

Q.3 Do OR, AND, NOT, EXOR, ExNOR for make these gate by NAND and NOR

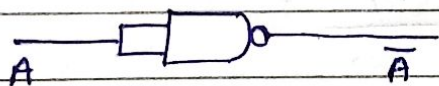
Ans (1) A



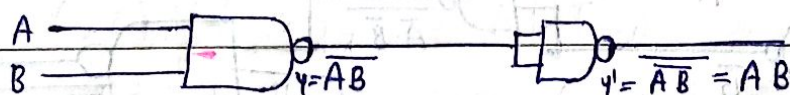
Ans (2)



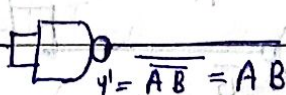
Ans (3) (i) NAND to NOT $\Rightarrow$



(ii)

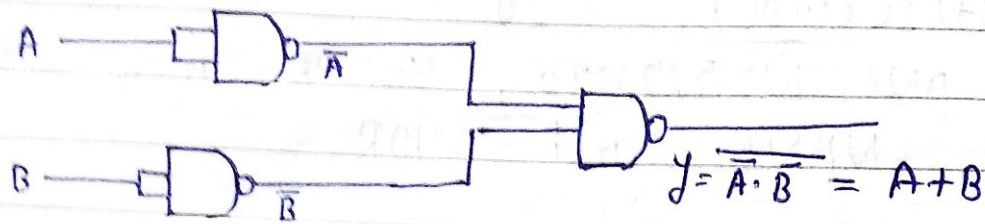


NAND to AND $\Rightarrow$

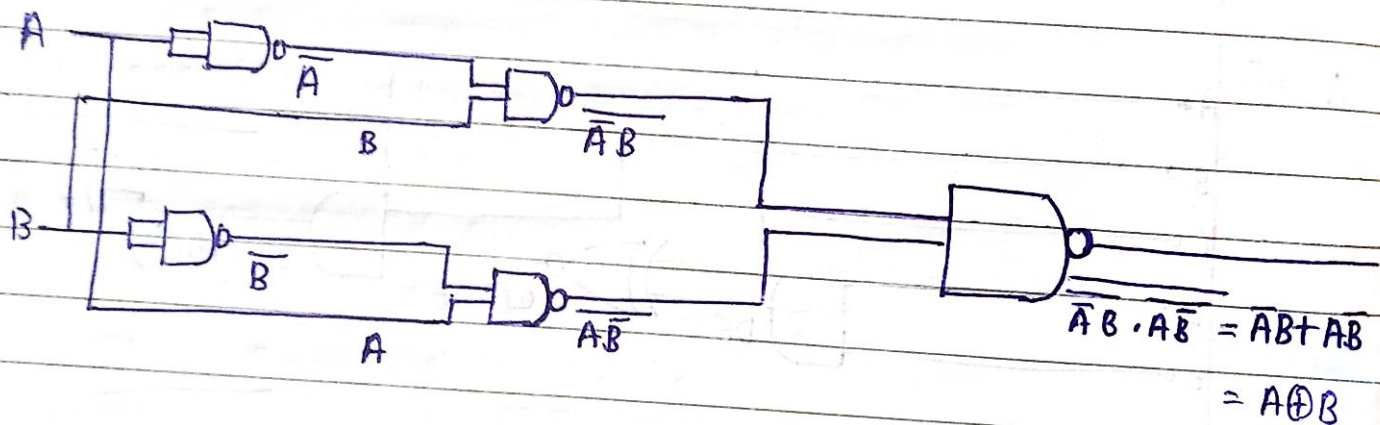
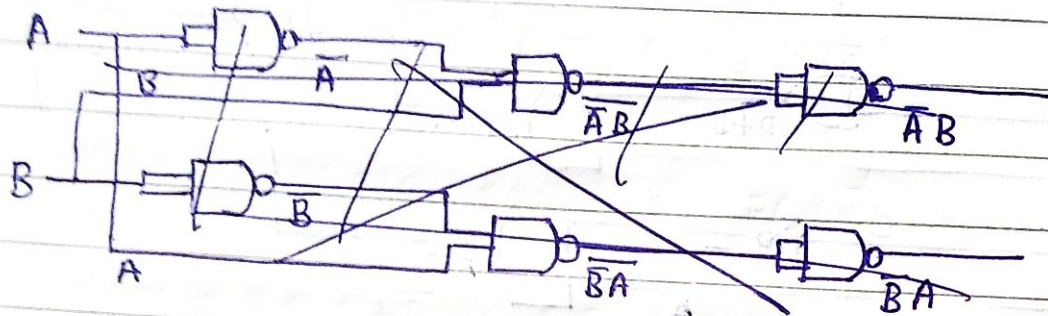


$$\left\{ \begin{array}{l} A=1 \\ B=1 \end{array} \right\} \quad \left\{ \begin{array}{l} y = \overline{1 \cdot 1} = \overline{1} = 0 \\ y' = \overline{0} = 1 \end{array} \right\}$$

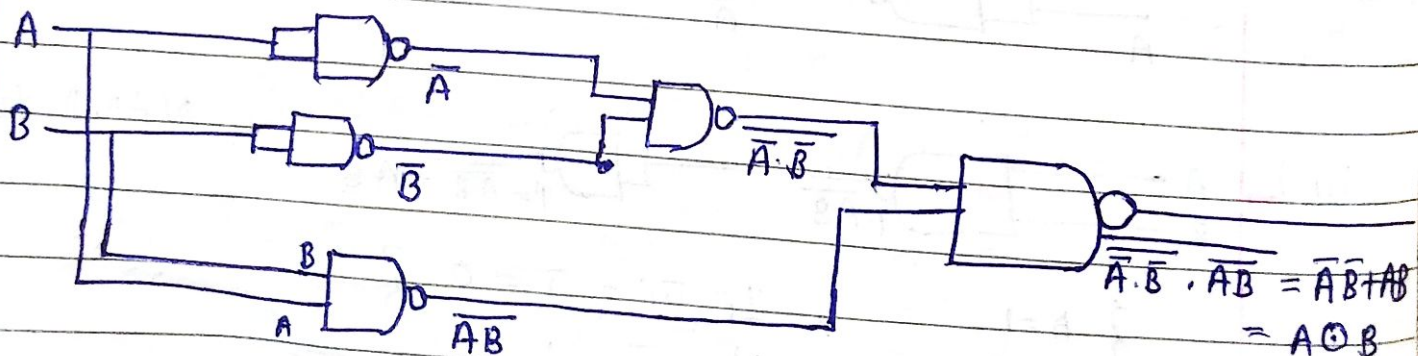
(C) NAND to OR Gate $\Rightarrow$



(D) NAND to Ex-OR Gate $\Rightarrow$



(E) NAND to Ex-NOR $\Rightarrow$

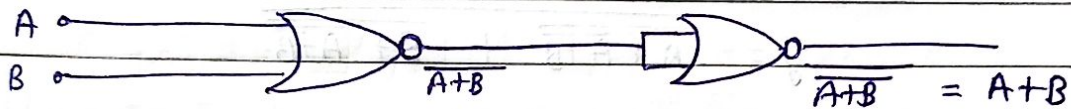


$$\left. \begin{aligned} \therefore \bar{A} \cdot \bar{B} &= \overline{A+B} \\ \bar{A} + \bar{B} &= \overline{A \cdot B} \end{aligned} \right\} \text{POPU}$$

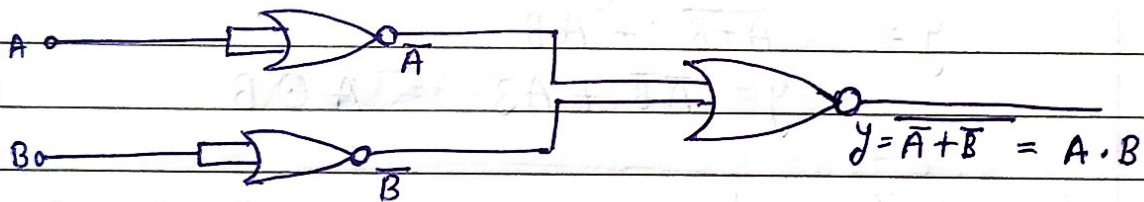
(A) NOR to NOT $\Rightarrow$



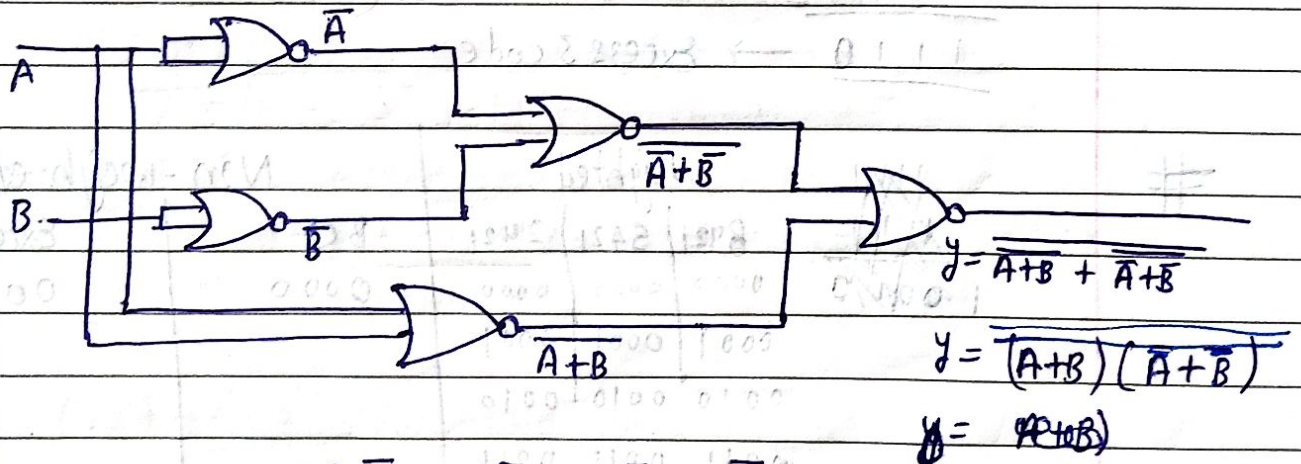
(B) NOR to OR $\Rightarrow$



(C) NOR to AND $\Rightarrow$



(D) NOR to EXOR Gate $\Rightarrow$

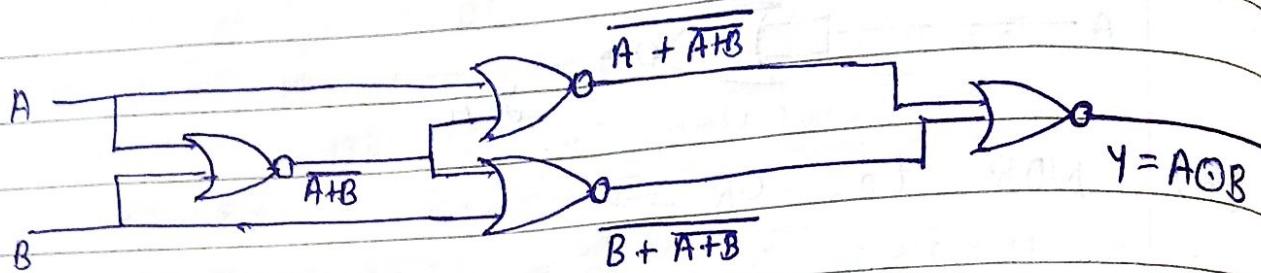


$$y = A\bar{A} + A\bar{B} + B\bar{A} + B\bar{B}$$

$$y = A\bar{B} + B\bar{A}$$

$$y = (A+B)$$

(E) NOR to Ex-NOR Gate $\Rightarrow$



$$Y = \overline{A + A + B} + \overline{B + A + B}$$

$$Y = (A + \overline{A+B}) (B + \overline{A+B})$$

$\{ \because \text{Transportation Theorem} \}$

$$(A+B)(A+B) = A + B$$

$$Y = \overline{A+B} + AB$$

$$Y = \overline{A+B} + AB = A \odot B$$

Excess 3 code $\Rightarrow$

It works 0 to 9.

Q.

$$\begin{array}{r} 1011 \\ 0011 \\ \hline 1110 \end{array} \rightarrow \text{Excess 3 code}$$

#

~~10010~~

Weighted

8421	5421	2421
0000	0000	0000
0001	0001	0001
0010	0010	0010
0011	0011	0011
0100	0100	0100
0101	1000	0101

Non-weighted

BCD
0000

Excess-3
0011

~~Boolean~~ Boolean Logic operation $\Rightarrow$

Addition	Multi
$0+0=0$	$0 \cdot 0=0$
$0+1=1$	$0 \cdot 1=0$
$1+0=1$	$1 \cdot 0=0$
$1+1=1$	$1 \cdot 1=1$

Basic Law of Boolean Algebra:—

Property

(i)

Commutative property:—

$$A+B = B+A$$

$$A \cdot B = B \cdot A$$

(ii)

Associative property:—

$$A+(B+C) = (A+B)+C$$

$$A \cdot (B \cdot C) = (A \cdot B) \cdot C$$

(iii)

Distributive property:—

$$A+BC = (A+B)(A+C)$$

$$A \cdot (B+C) = AB+AC$$

(iv)

Absorption ~~property~~ Law:—

(a)

$$A+AB = A \Rightarrow A(1+B) = A$$

(b)

$$A \cdot (A+B) = A$$

(c)

$$A+\bar{A}B = A+B \Rightarrow (A+\bar{A})(A+B) = A+B$$

(d)

$$A \cdot (\bar{A}+B) = AB$$

(v)

Consensus Law:—

$$AB + \bar{A}C + BC = AB + \bar{A}C$$

$$(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$$

(vi) Boolean Law :-

(a) $A + A = A$

(b) $A + 0 = A$

(c) $A + 1 = 1$

(d) $A + \bar{A} = 1$

(e) $A \cdot A = A$

(f) $A \cdot 0 = 0$

(g) $A \cdot 1 = A$

(h) $A \cdot \bar{A} = 0$

(i) $\bar{\bar{A}} = A$

Q. LHS = $AB + \bar{A}C + BC = AB + \bar{A}C$
 $= AB + \bar{A}C + BC \cdot 1$
 $= AB + \bar{A}C + BC(A + \bar{A})$
 $= AB + \bar{A}C + ABC + \bar{A}BC$
 $= AB(1 + C) + \bar{A}C(1 + B)$
 $= AB + \bar{A}C$ ✓

$\because A + \bar{A} = 1$
 $\because B + 1 = 1$
 $\because C + 1 = 1$

Q. Soln:- $(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$

$(A+B)(\bar{A}+C)(B+C)(A+\bar{A})$
 $(A\bar{A} + AC + \bar{A}B + BC)(AB + \bar{A}B + AC + \bar{A}C)(A\bar{A})$
 $(\bar{A}(A+B) + C(A+B))(\bar{A}(A+B) + C(A+\bar{A}) + AB)$
 $(A+B)(B+C)(\bar{A}+C)$
 $(A+\bar{A})(B+AC)(\bar{A}+C)$
 $(AB + AC + \bar{A}B)(\bar{A}+C)$
 $(B(A+\bar{A}) + AC)(\bar{A}+C)$
 $(AB + AC + \bar{A}B + A\bar{A})(\bar{A}+C)$
 $(\bar{A}(A+B) + A(B+C))(\bar{A}+C)$

Q. $(A+B)(\bar{A}+C)(B+C) = (A+B)(\bar{A}+C)$

Soln:- LHS

$(A+B)(\bar{A}+C)(B+C+A)$
 $(A+B)(\bar{A}+C)(B+C+A\bar{A})$
 $(A+B)(\bar{A}+C)(B+C+A)(B+C+\bar{A})$
 $(A+B)(A+B+C)(\bar{A}+C)(\bar{A}+B+C)$
 $((A+B)(A+B) + (A+B) \cdot C)((\bar{A}+C)(\bar{A}+C) + (\bar{A}+C) \cdot B)$

$$\begin{aligned}
 & ((A+B) + (A+B) \cdot C) = ((\bar{A}+C) + (\bar{A}+C) \cdot B) \\
 & ((A+B)(1+C)) = ((\bar{A}+C)(1+B)) \\
 & ((A+B)(1)) = ((\bar{A}+C)(1)) \\
 & = (A+B)(\bar{A}+C)
 \end{aligned}$$

Q.1 $AB + BC + \bar{B}C = AB + C$

Q.2 $\bar{A}B + AB + \bar{A}\bar{B}$

Q.3 $A + A\bar{B} + \bar{A}B$

Q.4 $(\bar{A}B + C\bar{D}) = (A + \bar{B})(C + D)$

Ans-1 LHS $AB + BC + \bar{B}C$
 $AB + C(B + \bar{B})$
 $AB + C \cdot 1$
 $AB + C = \text{RHS}$

Ans-2 $\bar{A}B + AB + \bar{A}\bar{B}$
 $B(A + \bar{A}) + \bar{A}\bar{B}$
 $B \cdot 1 + \bar{A}\bar{B}$
 $B + \bar{A}\bar{B}$
 $(B + \bar{A})(B + \bar{B})$
 $= \bar{A} + B$ { $\because A + \bar{A} = 1$ }

Ans-3 $A + A\bar{B} + \bar{A}B$
 $A(1 + \bar{B}) + \bar{A}B$
 $A \cdot 1 + \bar{A}B$
 $A + \bar{A}B$
 $(A + B)(A + \bar{A})$
 $= A + B$ { $A + B = (A + B)(A + C)$ }

$$\left\{ \begin{array}{l} \overline{A \cdot B} = \overline{A+B} \\ \overline{\overline{A+B}} = \overline{A+B} \end{array} \right\}$$

$$\overline{\overline{A+B}} = \overline{A+B}$$

POPU

Date: / /

Q. 4

$$(\overline{AB+CD}) = (A+B)(\overline{C+D})$$

LHS

$$\begin{aligned} \overline{AB+CD} &= \overline{(\overline{A+B})(\overline{C+D})} \quad \left\{ \begin{array}{l} \because \overline{AB} = \overline{A+B} \\ \therefore \overline{CD} = \overline{C+D} \end{array} \right\} \\ &= \overline{A+B} + \overline{C+D} \\ &= \overline{AB} \cdot \overline{CD} \\ &= (\overline{A+B})(\overline{C+D}) \\ &= (A+B)(\overline{C+D}) = \text{RHS} \end{aligned}$$

Q.

Ans -

$$\begin{aligned} &AB + \overline{AC} + A\overline{B}C \quad (AB+C) \\ &AB + \overline{A+C} + A\overline{B}C \cdot AB + A\overline{B}C \cdot C \\ &= AB + \overline{A+C} + A\overline{B}C \\ &= \overline{A+B} + (\overline{C+C})(\overline{C+AB}) \\ &= \overline{A+B} + \overline{C+AB} \\ &= \overline{A+C} + \overline{B+AB} \\ &= \overline{A+C} + (\overline{B+B})(\overline{A+B}) \\ &= \overline{A+C} + \overline{A+B} \\ &= \overline{C+B+1} \\ &= \overline{C+1} \\ &= 1 \end{aligned}$$

Q.

Ans -

$$(\overline{AB+C})(\overline{A+B+C})$$

$$(\overline{AB+C})(\overline{A+B+C})$$

$$= \overline{AB \cdot \overline{AB} + ABC + \overline{A}\overline{B}\overline{C} + C\overline{C}}$$

$$= \overline{ABC + \overline{A}\overline{B}\overline{C}} = (\overline{ABC}) \cdot (\overline{\overline{A}\overline{B}\overline{C}})$$

$$= (\overline{ABC})(\overline{\overline{A+B+C}})$$

$$= (A+B+C)(\overline{A+B+C})$$

Q.1 $(\bar{A} + B)(A + B)$

Q.2 $\overline{A\bar{B} + ABC} + A(B + A\bar{B})$

Ans-1 $(\bar{A} + B)(A + B)$

$$A\bar{A} + \bar{A}B + AB + B \cdot B$$

$$\{A\bar{A} = 0, B \cdot B = B\}$$

$$\bar{A}B + AB + B$$

$$\bar{A}B + B(A+1)$$

$$\{ \because A+1=1 \}$$

$$\bar{A}B + B$$

$$B(\bar{A}+1)$$

$$\{ \because \bar{A}+1=1 \}$$

$$= B$$

Ans

Ans-2 $\overline{A\bar{B} + ABC} + A(B + A\bar{B})$

$$\overline{A\bar{B} \cdot \overline{ABC}} + AB + A \cdot \overline{A\bar{B}} = (\bar{A} + B)(\bar{A} + \bar{B} + \bar{C}) + AB + \overline{A\bar{B}}$$

$$= \bar{A} \cdot \bar{A} + \bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{C} + \bar{A}B + B\bar{B} + B\bar{C} + A(B + \bar{B})$$

$$= \bar{A} + \bar{A}(\bar{B} + \bar{C}) + B(\bar{B} + \bar{C}) + \bar{A}B + A$$

$$= \bar{A} + (\bar{A} + B)(\bar{B} + \bar{C}) + A + B$$

$$= \bar{A} \cdot (\bar{A} + B)(\bar{B} + \bar{C}) + A + B$$

$$= (A) \{ \overline{\bar{A} + B} + \overline{\bar{B} + \bar{C}} \} (\bar{A} \cdot \bar{B})$$

$$= A (A \cdot \bar{B} + BC) (\bar{A} \bar{B})$$

$$= (\bar{A}\bar{B} + ABC) \bar{A}\bar{B} = \bar{A}\bar{A}\bar{B}\bar{B} + \bar{A}\bar{A} \cdot B\bar{B}C = 0$$

Principle of Duality

Boolean	Law S
(a)	(b)
$A+0=A$	$A \cdot 1=A$
$A+1=1$	$A \cdot 0=0$
$A+A=A$	$A \cdot A=A$
$A+\bar{A}=1$	$A \cdot \bar{A}=0$

$$\left\{ \begin{array}{l} 0 \rightarrow + \\ + \rightarrow 0 \\ 1 \rightarrow \cdot \\ \cdot \rightarrow 1 \end{array} \right\}$$

From the above properties and Law of Boolean algebra it is evident that they are group 0 where a & b. One expression can be obtained from the other in each pair by replacing every 1 with 0, every 0 with 1 and every +ve with $\cdot$ and every $\cdot$ with +ve. Any pair of expression satisfy this properties is called dual expression. This characteristic of boolean algebra is called principle of duality.

De - Morgan's theorem $\Rightarrow$

$$\overline{AB} = \overline{A} + \overline{B}$$

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

Minimization of Boolean Expression $\Rightarrow$

Q.1 $A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D$

Q.2 $(A+B)(\bar{A}\bar{C}+C)(\overline{B+AC})$

Ans-1

$$A + \bar{A}B + \bar{A}\bar{B}C(1+D)$$

$$A + \bar{A}B + \bar{A}\bar{B}C$$

$$A + B + \bar{A}\bar{B}C$$

$$A + B + \bar{B}\bar{A}C$$

$$A + (B+\bar{B})(B+\bar{A}C)$$

$$A + B + \bar{A}C$$

$$(A+\bar{A})(A+C) + B$$

=

$$A+B+\bar{C}$$

Ans-2 $(A+B)C$

Ans-1

$$A + \bar{A}B + \bar{A}\bar{B}(C+\bar{C}D)$$

$$A + \bar{A}B + \bar{A}\bar{B}(C+D)$$

$$A + B + \bar{A}\bar{B}C + \bar{A}\bar{B}D$$

$$A + \bar{A}\bar{B}D + B + \bar{B}\bar{A}C$$

$$(A+\bar{A})(A+\bar{B}D) + (B+\bar{B})(B+\bar{A}C)$$

$$A + \bar{B}D + B + \bar{A}C$$

$$A + \bar{A}C + (B+\bar{B})(B+D)$$

$$(A+\bar{A})(A+C) + (B+\bar{B})(B+D)$$

$$= A+B+(C+D)$$

Ans-2

=

$$(A+B)(\bar{A}\bar{C}+C)(\overline{B+AC})$$

$$(A+B)(C+\bar{C})(C+\bar{A})(\bar{B} \cdot \bar{A}C)$$

$$(A+B)(\bar{A}+C)(B \cdot (\bar{A}+\bar{C}))$$

$$(A\bar{A} + AC + \bar{A}B + BC) \cdot (\bar{A}B + B\bar{C})$$

$$(AC + \bar{A}B + BC)(\bar{A}B + B\bar{C})$$

$$AC \cdot \bar{A}B + AC \cdot B\bar{C} + \bar{A}B \cdot \bar{A}B + \bar{A}B \cdot B\bar{C} + BC \cdot \bar{A}B + BC \cdot B\bar{C}$$

$$0 + 0 + \bar{A}B + \bar{A}\bar{C}B + \bar{A}CB + 0$$

$$= \bar{A}B + \bar{A}\bar{C}B + \bar{A}CB$$

$$\begin{aligned} \overline{A}B(c+\overline{c}) + \overline{A}B \\ = \overline{A}B + \overline{A}B \\ = \overline{A}B \end{aligned}$$

Q. If $\overline{A}B + c\overline{D} = 0$ then prove that

$$\overline{A}B + \overline{c}(\overline{A} + \overline{D}) = AB + BD + \overline{B}\overline{D} + \overline{A}\overline{C}\overline{D}$$

Ans - LHS :-

$$\begin{aligned} \overline{A}B + \overline{c}(\overline{A} + \overline{D}) + 0 \\ \overline{A} + \overline{B} + \overline{A}\overline{c} + \overline{c}\overline{D} \\ \overline{A} + \overline{B} + \overline{A} + \overline{c} + \overline{c} + \overline{D} \\ (\overline{A} + \overline{B})(\overline{A} + \overline{c})(\overline{c} + \overline{D}) \end{aligned}$$

$$\begin{aligned} (\overline{A} + \overline{B} + \overline{A}\overline{c})\overline{c} \\ \overline{A}\overline{c} + \overline{A}\overline{B}\overline{c} \end{aligned}$$

$$\begin{aligned} AB + \overline{c}(\overline{A} + \overline{D}) + \overline{A}B + \overline{c}\overline{D} \\ AB + \overline{A}B + \overline{A}\overline{c} + \overline{c}\overline{D} + \overline{c}\overline{D} \\ B + \overline{A}\overline{c} + \overline{c}\overline{D} + \overline{c}\overline{D} \\ B + \overline{c}(\overline{A} + \overline{D}) + \overline{c}\overline{D} + \overline{A}\overline{c} \end{aligned}$$

$$\begin{aligned} \text{RHS} = AB + BD + \overline{B}\overline{D} + \overline{A}\overline{C}\overline{D} + 0 \\ AB + BD + \overline{B}\overline{D} + \overline{A}\overline{C}\overline{D} + \overline{A}B + \overline{c}\overline{D} \\ B + \overline{D}(\overline{B} + \overline{c}) + (\overline{A}\overline{c} + \overline{B})\overline{D} + \overline{A}B \\ B(1 + \overline{A}) + \overline{D}(\overline{B} + \overline{c}) + \overline{D}(\overline{A}\overline{c} + \overline{B}) \\ B + \overline{B}\overline{D} + \overline{c}\overline{D} + \overline{A}\overline{C}\overline{D} + BD \\ B + BD + \overline{B}\overline{D} + \overline{c}\overline{D} + \overline{A}\overline{C}\overline{D} \\ B + \overline{B}\overline{D} + \overline{c}\overline{D} + \overline{A}\overline{C}\overline{D} \\ B + \overline{D} + \overline{c}\overline{D} + \overline{A}\overline{C}\overline{D} \\ B + \overline{D}(1 + \overline{c}) + \overline{A}\overline{C}\overline{D} \\ B + \overline{D} + \overline{A}\overline{C}\overline{D} \\ B + (\overline{D} + \overline{D})(\overline{D} + \overline{A}\overline{C}) \end{aligned}$$

$$\begin{aligned} B + \overline{D} + \overline{A}\overline{C} \\ \text{LHS} = \text{RHS} \end{aligned}$$

SOP & POS [Sum of product & product of sum]
 $\Rightarrow$

(i) ~~Product~~ $\Rightarrow$ The ~~and~~ ^{AND} function is referred to as a product - in Boolean algebra
~~the word product.~~ eg - $A \cdot B$

(ii) Sum $\Rightarrow$ An ~~or~~ ^{OR} function is referred to as a sum.
 eg - $A + B$

(iii) Sum of Product (SOP) $\Rightarrow$ The logical sum of two or more logical product term is called a SOP. $Y = AB + BC + ABC$ It is basically an OR operation of product terms.

(iv) Product of Sum (POS) $\Rightarrow$
 $Y = (A+B)(B+C)(A+B+C)$

It is basically an OR operation of AND operation variables.

A product of sum expression is a logical product of two or more logical sum term. It is basically an AND operation of OR operated variable such as

Minterm $\Rightarrow$ $\left. \begin{matrix} A=1 \\ \bar{A}=0 \end{matrix} \right\}$

A	B	C	Minterm	
0	0	0	$\bar{A} \cdot \bar{B} \cdot \bar{C}$	m_0
0	0	1	$\bar{A} \cdot \bar{B} \cdot C$	m_1
0	1	0	$\bar{A} \cdot B \cdot \bar{C}$	m_2
0	1	1	$\bar{A} B C$	m_3
1	0	0	$A \bar{B} \bar{C}$	m_4
1	0	1	$A \bar{B} C$	m_5
1	1	0	$A B \bar{C}$	m_6
1	1	1	$A B C$	m_7

SOP

$$\begin{cases} A \rightarrow 0 \\ \bar{A} = 1 \end{cases}$$

Maxterm $\Rightarrow$			Maxterm	
A	B	C		
0	0	0	$A+B+C$	M_0
0	0	1	$A+B+\bar{C}$	M_1
0	1	0	$A+\bar{B}+C$	M_2
0	1	1	$A+\bar{B}+\bar{C}$	M_3
1	0	0	$\bar{A}+B+C$	M_4
1	0	1	$\bar{A}+B+\bar{C}$	M_5
1	1	0	$\bar{A}+\bar{B}+C$	M_6
1	1	1	$\bar{A}+\bar{B}+\bar{C}$	M_7

POS
 Π

Canonical SOP $\Rightarrow$

Q.

$$Y = \sum m(0, 5, 6)$$

$$Y = \sum (m_0, m_5, m_6)$$

$$Y = m_0 + m_5 + m_6$$

$$Y = \bar{A} \cdot \bar{B} \cdot \bar{C} + A \cdot \bar{B} \cdot C + A \cdot B \cdot \bar{C}$$

Obtain the canonical SOP from the given function:—

Q.

$$Y(A, B, C) = A + BC$$

$$= A \cdot 1 \cdot 1 + BC \cdot 1$$

$$= A(B+\bar{B})(C+\bar{C}) + BC(A+\bar{A})$$

$$= (AB + A\bar{B})(C + \bar{C}) + ABC + \bar{A}BC$$

$$= ABC + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}B\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$$

$$= ABC + \bar{A}BC + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}$$

$$= m_7 + m_3 + m_5 + m_6 + m_4$$

$$Y = \sum m(3, 4, 5, 6, 7)$$

CPOS $\Rightarrow$

CPOS

000 $\rightarrow$ $A+B+C$
010

Q.

$$Y = \prod_m (0, 2, 4, 7)$$

$$Y = M_0 \cdot M_2 \cdot M_4 \cdot M_7$$

$$Y = (A+B+C) \cdot (A+\bar{B}+C) \cdot (\bar{A}+B+C) \cdot (\bar{A}+\bar{B}+\bar{C})$$

$$Y = (A \cdot A + A\bar{B} + AC + AB + A\bar{C} + B\bar{B} + BC + \bar{B}C + C \cdot C) \cdot (\bar{A} \cdot \bar{A} + \bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{C} + B\bar{B} + \bar{A}B + B\bar{C} + \bar{A}C + \bar{B}C + C\bar{C})$$

$$Y = (A + A\bar{B} + AB + AC + B\bar{C} + \bar{B}C + C) (\bar{A} + \bar{A} \cdot \bar{B} + \bar{A} \cdot \bar{C} + \bar{A}B + B\bar{C} + \bar{A}C + \bar{B}C + C)$$

$$Y = (A + A + C + AC) (\bar{A} + \bar{A} + \bar{A} + B\bar{C} + \bar{B}C)$$

$$Y = (A + C + AC) (\bar{A} + B\bar{C} + \bar{B}C)$$

Obtain CPOS: —

Q.

$$Y = (A+\bar{B})(B+C)(A+\bar{C})$$

$$Y = (A+\bar{B}+0)(B+C+0)(A+\bar{C}+0)$$

$$Y = (A+\bar{B}+C \cdot \bar{C})(B+C+A\bar{A})(A+\bar{C}+B \cdot \bar{B})$$

$$Y = (A+\bar{B}+C)(A+\bar{B}+\bar{C})(B+C+A)(B+C+\bar{A})(A+\bar{C}+B)(A+\bar{C}+\bar{B})$$

$$Y = (A+\bar{B}+\bar{C})(\bar{A}+B+C)(A+\bar{B}+C)(A+B+\bar{C})(A+B+C)$$

$$Y = M_3 \cdot M_4 \cdot M_2 \cdot M_1 \cdot M_0$$

$$Y = \prod (0, 1, 2, 3, 4)$$

$$Y(A, B, C) = \prod (0, 1, 2, 3, 4)$$

Q. $Y = A + \bar{B}C$

(a) CPOS (b) CSOP

Ans (b) CSOP :-

$$\begin{aligned} Y(A, B, C) &= A \cdot 1 \cdot 1 + \bar{B}C(1) \\ &= A(B + \bar{B})(C + \bar{C}) + \bar{B}C(A + \bar{A}) \\ &= (AB + A\bar{B})(C + \bar{C}) + A\bar{B}C + \bar{A}\bar{B}C \\ &= ABC + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} \\ Y &= ABC + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} \\ &\quad \cancel{ABC + A\bar{B}\bar{C} + \bar{B}C(A + \bar{A})} \end{aligned}$$

$$Y = m_7 + m_5 + m_4 + m_1 + m_0$$

$$Y = \sum_m (1, 4, 5, 7)$$

(a) CPOS :-

$$Y(A, B, C) = (A + \bar{B}C)$$

$$Y(A, B, C) = (A + C)(A + \bar{B})$$

$$= (A + C + 0)(A + \bar{B} + 0)$$

$$Y = (A + C + B\bar{B})(A + \bar{B} + C\bar{C})$$

$$Y = (A + C + B)(A + C + \bar{B})(A + \bar{B} + C)(A + \bar{B} + \bar{C})$$

$$Y = (A + B + C)(A + \bar{B} + C)(A + \bar{B} + \bar{C})$$

$$Y = M_0 \cdot M_2 \cdot M_3$$

$$Y = \prod (0, 2, 3)$$

Karnaugh Map (K-Map)

2-Variable :-

A \ B	0	1
0	0	1
1	2	3

3- Variable :-

A	BC			
	00	01	11	10
0	0	1	3	2
1	4	5	7	6

A	BC			
	00	01	11	10
0	0	1	3	2
1	4	5	7	6

C	AB			
	00	01	11	10
0	0	2	6	4
1	1	3	7	5

AND gate prove by K-Map

A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

A	B
0	0
0	1
1	0
1	1

↓ AB

OR gate prove by K-Map

A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

A	B
0	0
0	1
1	0
1	1

① → A(B + $\bar{B}$) = A
 ② → B(A + $\bar{A}$) = B
 Y → ① + ②
 Y → A + B

NAND gate prove by using K-Map :-

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

A	B
0	0
0	1
1	0
1	1

① → $\bar{B}$
 ② → $\bar{A}$
 Y = $\bar{A} + \bar{B} = \overline{AB}$

NOR gate prove by using K-Map

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

A \ B	0	1
0	1	0
1	0	0

$$Y = \overline{A \cdot B} = \overline{A + B}$$

Ex-OR :-

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A \ B	0	1
0	0	1
1	1	0

$$\textcircled{1} \rightarrow \overline{A} \overline{B}$$

$$\textcircled{2} \rightarrow B \overline{A}$$

$$Y = \overline{A} \overline{B} + B \overline{A} = A \oplus B$$

Ex-NOR :-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

A \ B	0	1
0	1	0
1	0	1

$$Y = \overline{A} \overline{B} + AB = A \odot B$$

3 variable :-

Q.

Ans-

$Y = \sum m(0, 1, 2, 4, 5)$ solve using K-Map

$$Y = m_0 + m_1 + m_2 + m_4 + m_5$$

$$Y = \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} C + \overline{A} B \overline{C} + A \overline{B} \overline{C} + A \overline{B} C$$

A \ BC	00	01	11	10
0	1	1	0	1
1	1	1	0	0

$$\textcircled{10} \rightarrow \bar{B}\bar{C} + \bar{B}C + \bar{A} + A + \bar{A}\bar{B}$$

$$\textcircled{1} \rightarrow \bar{B}\bar{C}$$

$$\textcircled{2} \rightarrow \bar{B}C$$

$$\textcircled{3} \rightarrow \bar{A}\bar{B}$$

$$\textcircled{4} \rightarrow A\bar{B}$$

$$\textcircled{5} \rightarrow \bar{A}B\bar{C}$$

$$Y = \bar{B}\bar{C} + \bar{B}C + \bar{A}\bar{B} + A\bar{B} + \bar{A}B\bar{C}$$

$$Y = \bar{B}(C + \bar{C}) + \bar{B}(A + \bar{A}) + \bar{A}B\bar{C}$$

$$Y = \bar{B} + \bar{B} + \bar{A}B\bar{C}$$

$$Y = \bar{B} + \bar{A}B\bar{C}$$

$$Y = (\bar{B} + \bar{B})(\bar{B} + \bar{A}\bar{C})$$

$$Y = \bar{B} + \bar{A}\bar{C}$$

011

A \ BC	00	01	11	10
0	1	1		1
1	1	1		

① → (row 0)
② → (col 1)

Consider maximum pair and take corner also.

$$\textcircled{1} \rightarrow \bar{B}$$

$$\textcircled{2} \rightarrow \bar{A}\bar{C}$$

$$Y = \bar{B} + \bar{A}\bar{C} \quad \underline{Ans}$$

Q.

$$Y = \sum m(0, 1, 2, 3, 4, 5, 6, 7)$$

Ans -

A \ BC	00	01	11	10
0	1	1	1	1
1	1	1	1	1

① → (all cells)

$$\bar{B}(0) + B(0) \quad Y = 1 \quad \underline{Ans}$$

4-Variable $\Rightarrow$

8421

AB \ CD	00	01	11	10
00	0	1	1	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

① $\rightarrow$ BD

② $\rightarrow \bar{A} \bar{B} \bar{C}$

③ $\rightarrow ABC$

④ $\rightarrow \bar{A} \bar{C} D$

⑤ $\rightarrow A \bar{C} D$

Q.

Ans -

$$Y = \sum m(3, 4, 5, 7, 9, 13, 14, 15)$$

AB \ CD	00	01	11	10
00	0	1	1	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

① $\rightarrow$ BD

② $\rightarrow \bar{A} \bar{B} \bar{C} \bar{D}$

② $\rightarrow \bar{A} \bar{B} \bar{C}$

③ $\rightarrow \bar{A} \bar{B} C \bar{D}$

③ $\rightarrow ABC$

④ $\rightarrow \bar{A} \bar{B} C D$

④ $\rightarrow A \bar{C} \bar{D}$

⑤ $\rightarrow \bar{A} \bar{B} C D$

⑤ $\rightarrow \bar{A} C D$

$$Y = BD + \bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} C + A \bar{C} \bar{D} + \bar{A} C D \checkmark$$

H.W.

Q. 1

Q. 2

Ans - 1

$$Y = m_1 + m_5 + m_{10} + m_{11} + m_{12} + m_{13} + m_{15}$$

$$Y = \sum m(8, 10, 11, 12, 13, 14, 15)$$

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

$$\textcircled{1} \rightarrow \bar{A}\bar{C}D$$

$$\textcircled{2} \rightarrow A\bar{B}\bar{C}$$

$$\textcircled{3} \rightarrow ACD$$

$$\textcircled{4} \rightarrow A\bar{B}C$$

$$\textcircled{1} = \textcircled{8} \rightarrow \bar{A}\bar{C}D$$

$$\textcircled{2} = \textcircled{7} \rightarrow A\bar{B}\bar{C}$$

$$\textcircled{4} = \textcircled{5} \rightarrow A\bar{B}C$$

$$\textcircled{6} \rightarrow ABD$$

$$Y = \textcircled{1} + \textcircled{2} + \textcircled{3} + \textcircled{4}$$

$$Y = \bar{A}\bar{C}D + A\bar{B}\bar{C} + ABD + A\bar{B}C$$

$$Y = \bar{A}\bar{C}D + A\bar{B}\bar{C} + ACD + A\bar{B}C$$

Ans-2

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

Groupings:
 (1) $\rightarrow$ $\bar{A}\bar{B}\bar{D}$ (cells 0, 1, 8, 9)
 (2) $\rightarrow$ $\bar{A}CD$ (cells 3, 7, 11, 15)
 (3) $\rightarrow$ $A\bar{B}\bar{D}$ (cells 12, 13, 10, 14)

$$\textcircled{1} \rightarrow \bar{A}\bar{B}\bar{D}$$

$$\textcircled{2} \rightarrow \bar{A}CD$$

$$\textcircled{3} \rightarrow A\bar{B}\bar{D}$$

$$Y = \bar{A}\bar{B}\bar{D} + \bar{A}CD + A\bar{B}\bar{D}$$

$$Y = \bar{A}\bar{B}\bar{D} + AC + A\bar{D}$$

$$Y = \bar{A}\bar{D}(B+1) + AC$$

$$Y = \bar{A}\bar{D} + AC$$

$$Y = A(C + \bar{D})$$

Q. $f(A, B, C, D) = \sum m(0, 1, 2, 3, 5, 7, 8, 9, 11, 14)$

Ans -

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

Groupings:
 (1) $\rightarrow$ $\bar{A}\bar{B}\bar{D}$ (cells 0, 1, 8, 9)
 (2) $\rightarrow$ $\bar{A}D$ (cells 1, 3, 5, 7, 9, 11, 13, 15)
 (3) $\rightarrow$ $\bar{B}\bar{C}$ (cells 0, 1, 4, 5, 8, 9, 12, 13)
 (4) $\rightarrow$ $\bar{B}D$ (cells 1, 3, 5, 7, 9, 11, 13, 15)
 (5) $\rightarrow$ $ABCD$ (cells 3, 7, 11, 15)

$$\textcircled{1} \rightarrow \bar{A}\bar{B}\bar{D}$$

$$\textcircled{2} \rightarrow \bar{A}D$$

$$\textcircled{3} \rightarrow \bar{B}\bar{C}$$

$$\textcircled{4} \rightarrow \bar{B}D$$

$$\textcircled{5} \rightarrow ABCD$$

$$Y = \bar{A} \bar{B} \bar{D} + \bar{A} D + \bar{B} C + \bar{B} D + ABC \bar{D}$$

K-Map with Don't Care $\Rightarrow$

Q.1 $F = \sum m(1, 3, 7, 15) + d(0, 2, 5)$

Ans -

$1 = A$
 $0 = \bar{A}$

AB \ CD	00	01	11	10
00	d	1	1	d
01	4	d	5	6
11	12	13	15	14
10	8	9	11	10

① $\rightarrow \bar{A} \bar{B} \bar{D}$

② $\rightarrow \bar{A} D$

③ $\rightarrow BCD$

$F = \bar{A} \bar{B} \bar{D} + \bar{A} D + BCD + \bar{A} \bar{B} \bar{D}$

$\bar{A} (\bar{B} \bar{D} + D) + BCD$

$((\bar{D} + D) (\bar{B} + D)) (\bar{A}) + BCD$

$= \bar{A} \bar{B} + \bar{A} D + BCD + \bar{A} \bar{B} \bar{D}$

$\bar{A} D + BCD$

Q.2 $F(W, X, Y, Z) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 5)$

Ans -

WX \ YZ	00	01	11	10
00	d	1	1	d
01	4	d	5	6
11	12	13	15	14
10	8	9	11	10

① $\rightarrow YZ \bar{X}$

② $\rightarrow \bar{W} Z$

$$F = \bar{X}YZ + \bar{W}Z$$

Five-Variable K-Map:-

Q. $\Sigma m(3, 6, 7, 8, 10, 12, 14, 17, 19, 20, 21, 24, 25, 27, 28)$

eg -

DE \ ABC	000	001	011	010	110	111	101	100
00	0	4	12	8	24	28	20	16
01	1	5	13	9	25	29	21	17
11	3	7	15	11	27	31	23	19
10	2	6	14	10	26	30	22	18

Groupings: ① (12, 28), ② (8, 24), ③ (21, 17), ④ (20, 16), ⑤ (3, 7), ⑥ (2, 6)

① $\rightarrow B\bar{D}\bar{E}C$

② $\rightarrow \bar{A}B\bar{E}$

③ $\rightarrow \bar{C}E\bar{A}$

④ $\rightarrow A\bar{B}C\bar{D}$

⑤ $\rightarrow \bar{A}\bar{B}CD$

⑥ $\rightarrow \bar{A}\bar{B}DE$

$$Y = CB\bar{D}\bar{E} + \bar{A}B\bar{E} + A\bar{E}\bar{C} + A\bar{B}C\bar{D} + \bar{A}\bar{B}CD + \bar{A}\bar{B}DE$$

~~Quine~~ McClusky $\Rightarrow$

$\rightarrow$ 5-variable k-map with Don't care $\Rightarrow$

Q. $Y = \Sigma m(1, 5, 7, 13, 14, 15, 17, 18, 21, 22, 25, 29) + \Sigma d(6, 9, 19, 23, 30)$

Ans -

DE \ ABC	000	001	011	010	110	111	101	100
00	0	4	12	8	24	28	20	16
01	1	5	13	d	25	29	21	17
11	3	7	15	11	27	31	d	19
10	2	d	6	10	26	d	22	18

Groupings: ① (17, 21), ② (18, 22), ③ (13, 15), ④ (14, 18), ⑤ (1, 5), ⑥ (7, 15), ⑦ (3, 7), ⑧ (2, 6)

① $\rightarrow \bar{B}\bar{C}\bar{D}E$

② $\rightarrow A\bar{B}D$

③ $\rightarrow \bar{A}C\bar{B}$

$$Y = \bar{B}\bar{C}\bar{D}E + A\bar{B}D + \bar{A}C\bar{B}$$

~~Quine McClusky~~

(Tabular method)

Quine McClusky $\Rightarrow$

Step-1 A set of all prime implicants of the function must be obtained

Step-2 From the set of all the prime implicants, a set of essential implicant must be determined by preparing a prime implicant chart.

Step-3 The minterm which are not covered by the essential implicants are taken into consideration and a minimum cover is obtained from the remaining prime implicants.

Q. $f = (1, 2, 3, 7, 8, 9, 10, 11, 14, 15)$

(a) Binary representation of Minterm: —

Minterm	Variable			
	A	B	C	D
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
14	1	1	1	0
15	1	1	1	1

(b) Groups of Minterm for different no. of 1's :—

No. of 1's	Minterm	Variables			
		A	B	C	D
1	1	0	0	0	1
	2	0	0	1	0
	8	1	0	0	0
2	3	0	0	1	1
	9	1	0	0	1
	10	1	0	1	0
3	7	0	1	1	1
	11	1	0	1	1
	14	1	1	1	0
4	15	1	1	1	1

Any 2 ~~input~~ no. in these groups which differ from each other by only 1 variable can be chose & combined to get 2 cell combination.

(c) Two cell combination :—

Combination	A	B	C	D
(1,3)	0	0	—	1
(1,9)	—	0	0	1
(2,3)	0	0	1	—
(2,10)	—	0	1	0
(8,9)	1	0	0	1
(8,10)	1	0	—	0
(3,7)	0	—	1	1
(3,11)	—	0	1	1
(9,11)	1	0	—	1
(10,11)	1	0	1	—

(10, 14)	1	-	1	0
(7, 15)	-	1	1	1
(11, 15)	1	-	1	1
(14, 15)	1	1	1	-

From the two cell combination one variable in one dash in the same position can be combined from 4 cell combination

(d) Four cell combination

Combination	A	B	C	D
(1, 3, 9, 11)	-	0	-	1
(0, 1, 3, 11)	0	0	-	1
(2, 3, 10, 11)	-	0	1	-
(2, 3, 14, 15)	-	0	1	-
(0, 1, 9, 11)	0	0	-	1
(8, 9, 10, 11)	1	0	-	-
(3, 7, 11, 15)	-	-	1	1
(10, 11, 14, 15)	1	-	1	-

$$f = \bar{B}D + \bar{B}C + A\bar{B} + CD + AC$$

(e) Prime Implicant Table: —

Prime implicant	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
(1, 3, 9, 11)	X	X							X		X				
(2, 3, 10, 11)		X	X							X	X				
(8, 9, 10, 11)								X	X	X	X				
(3, 7, 11, 15)		X					X				X				X
(10, 11, 14, 15)										X	X			X	X
	✓	✓					✓	✓						✓	

Q. $f(A, B, C, D) = \sum m(0, 1, 5, 7, 8, 10, 14, 15)$

*-
(a) Binary representation of Minterm: —

Minterm	Variable			
	A	B	C	D
0	0	0	0	0
1	0	0	0	1
5	0	1	0	1
7	0	1	1	1
8	1	0	0	0
10	1	0	1	0
14	1	1	1	0
15	1	1	1	1

(b) Group of minterm for different no. of 1's : —

No of 1's	Minterm	Variables			
		A	B	C	D
0	0	0	0	0	0
1	1	0	0	0	1
	8	1	0	0	0
2	5	0	1	0	1
	10	1	0	1	0
3	7	0	1	1	1
	14	1	1	1	0
4	15	1	1	1	1

Any 2 no. in these groups which differ from each other by only 1 variable can be chosen & combined to get 2 cell combination.

(c)

(d)

X

No match

(2)

[illegible]

~~Q. Q. Q.~~

$$f = \bar{A}\bar{B}\bar{C} + \bar{B}\bar{C}\bar{D} + \bar{A}\bar{C}\bar{D} + A\bar{B}\bar{D} + A\bar{B}D + A\bar{C}D + B\bar{C}D + ABC$$

Don't Carry in Tabular method:-

Q. $f(w, x, y, z) = (1, 3, 4, 5, 9, 10, 11) + \Sigma d(6, 8)$

Ans:-

(a) Binary representation of Minterms:-

Minterms	Variable			
	A	B	C	D
1	0	0	0	1
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1

(b) Group of minterm for different no. of 1's:-

No of 1's	Minterm	A	B	C	D
1	1	0	0	0	1
	8	1	0	0	0
	4	0	1	0	0
2	3	0	0	1	1
	5	0	1	0	1
	6	0	1	1	0
	9	1	0	0	1
	10	1	0	1	0
	11	1	0	1	1
3	11	1	0	1	1

(c) Two cell combination: -

Combination	A	B	C	D
(1,3)	0	0	-	1
(1,5)	0	-	0	1
(1,9)	-	0	0	1
(4,5)	0	1	0	-
(4,6)	0	1	-	0
(8,9)	1	0	0	-
(8,10)	1	0	-	0
(3,11)	-	0	1	1
(9,11)	1	0	-	1
(10,11)	1	0	1	-

(d) Four cell combination: -

Combination	A	B	C	D
(1,3,9,11)	-	0	-	1
(8,9,10,11)	1	0	-	-

(e) Prime Implicant Table: -

Prime implicant	1	3	4	5	9	10	11
(1,3,9,11)	x	x			x		x
(8,9,10,11)					x	x	x
(1,5)	x			x			
(4,5)			x	x			
(4,6)			x				
		✓				✓	

$$f(w, x, y, z) = \bar{x}z + w\bar{x} + \bar{w}x\bar{y}$$

(9, 4, 5)

Unit - III

Digital logic gate characteristic

Characteristics of digital IC $\Rightarrow$

- (i) Speed operation:— The speed operation of digital IC should be high. It is specified in terms of propagation delay time. It is the average of ~~the~~ propagation delay time from low to high & high to low state.

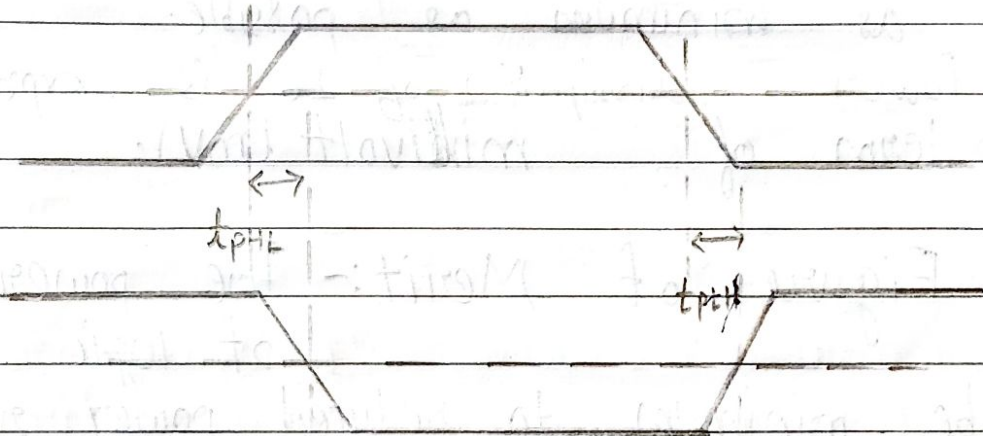


fig: Input & output wave form of logic gate

$$t_p = \frac{t_{pHL} + t_{pLH}}{2}$$

Where t_{pHL} is the delay time measured when output change from high to low state. And t_{pLH} is the delay time measured when output change from low to high state.

t_p = Propagation delay time

→ The delay time are measured b/w 50% of voltage level of i/p & o/p waveform.

The propagation delay b/w i/p & o/p should be as minimum as possible so that the operating speed of IC remains High.

(ii) **Power dissipation** :— Every electronic circuits require a certain amount of electric power for its operation. When the power is supplied by an external source some of it is dissipated in electronic ckt. It is wastage of power across the circuit component of IC. Requirement of power is less if the dissipation of power is less. Hence, power dissipation as minimum as possible. Power dissipation of IC is expressed in the term of millivolt (mV).

(iii) **Figure of Merit** :— The power dissipation of logic family should be minimum to reduced power requirement. But it is important to note that in logic families. If the power dissipation is reduced this speed of operation get reduce. Hence, the figure of merit is a parameter considered for comparison between instant using speed of operation & power dissipation. Figure of merit is product of propagation delay & power dissipation. It is measured in term of ~~ns~~ pico Jules (PJ)

$$\boxed{ns \times mW = PJ}$$

(iv) **Current & Voltage Parameter** :— V_{IH} (High level i/p voltage) $\Rightarrow$ It is minimum i/p voltage

corresponding to a logic ~~one~~ 1 state.

V_{IL} (low level i/p voltage) $\Rightarrow$ It is maximum i/p voltage corresponding to logic 0 state.

V_{OH} (High level o/p voltage) $\Rightarrow$ It is minimum o/p voltage corresponding to a logic 1 state.

V_{OL} (Low level o/p voltage) $\Rightarrow$ It is maximum o/p voltage corresponding to a logic 0 state.

I_{IH} (High level i/p current) $\Rightarrow$ It is minimum i/p current corresponding to a logic 1 state.

I_{IL} (Low level i/p current) $\Rightarrow$ It is maximum i/p current corresponding to a logic 0 state.

I_{OH} (High level o/p current) $\Rightarrow$ It is minimum o/p current corresponding to a logic 1 state.

I_{OL} (Low level o/p current) $\Rightarrow$ It is maximum o/p current corresponding to a logic 0 state.

(v) Fan out: —

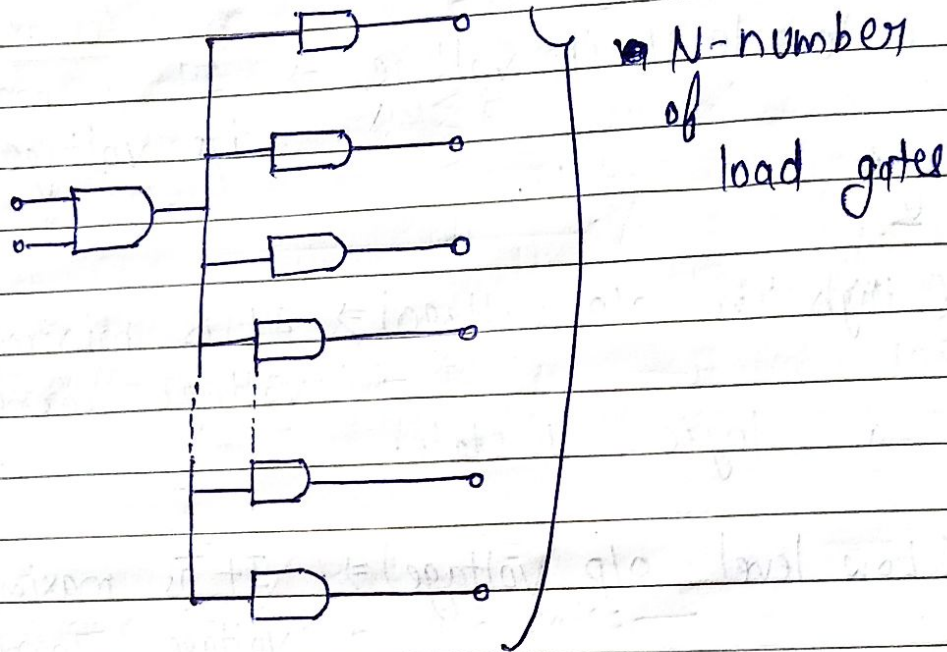


fig: AND gate driven N gates

Fan out is the capacity of a logic gate to drive the maximum no. similar gate.

High fan out is the better because it reduces need of additional gate to drive more gate.

$$F_{out} = \text{minimum} \left\{ \frac{I_{OH}}{I_{IH}}, \frac{I_{OL}}{I_{IL}} \right\}$$

(vi) Fan in: —

Fan in is the no. of i/p to a gate. For a two i/p gate, fan-in is 2. For a 4 i/p gate fan-in is 4.

(vii) Noise Immunity: —

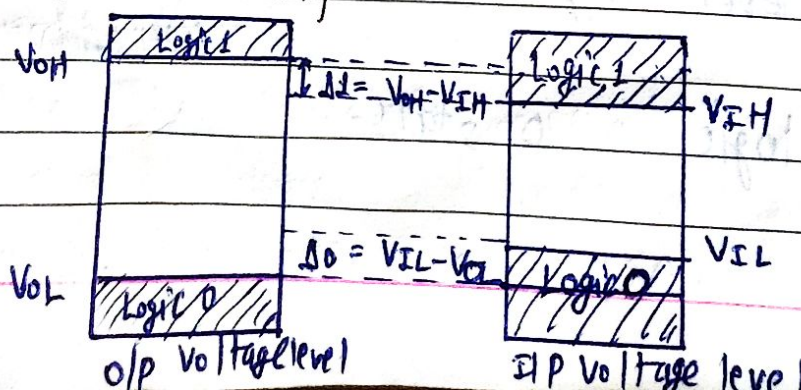


fig: i/p & o/p voltage level

Unwanted signals are known as noise. The noise immunity of digital circuit is defined as the ability of a digital circuit to tolerate the noise signal. A quantitative measure of noise immunity is known as noise margin.

Logic 1 state noise margin and 0 state noise margin can be calculated as :-

→ Logic 1 state noise margin $\Delta 1 = V_{OH} - V_{IH}$ (NM)

→ Logic 0 state noise margin $\Delta 0 = V_{IL} - V_{OL}$ (NM)

low noise margin

(viii) Power Supply requirement →

Every electronic circuit requires power supply to operate. The required supply voltage & power by the IC should be as less as possible.

(ix) Operating temperature → On the basis of the operating Temp. range the application of IC will be decided. The operating temp is the range of temp. in which an IC function properly.

It is in order of -55°C to $+125^{\circ}\text{C}$. The expected temp. range of an IC is 0 to 70°C for commercial & industrial

application. Selection of a particular logical family for a particular application depend of these parameter.

RTL (Resistor Transistor Logic) :-

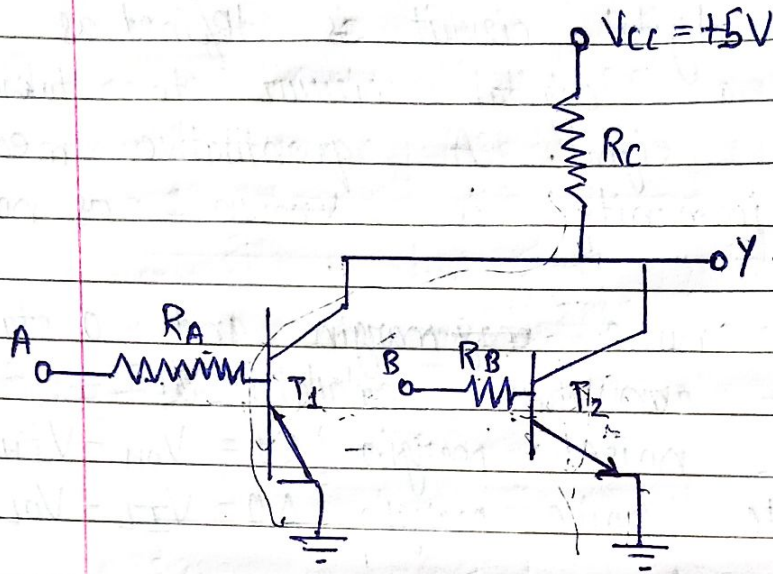


fig:-
Resistor transistor logic
NOR gate

Operation of RTL NOR gate:-

V_A	V_B	Transistor T_1	Transistor T_2	V_Y
Logic 0	Logic 0	Cutoff	Cutoff	Logic 1
Logic 0	Logic 1	Cutoff	Saturation	Logic 0
Logic 1	Logic 0	Saturation	Cutoff	Logic 0
Logic 1	Logic 1	Saturation	Saturation	Logic 0

RTL consists of resistor & Transistor. In RTL transistor operate in cutoff region & saturation region as per i/p voltage applied. In the figure shown the circuit of 2 i/p resistor transistor logic. Here A & B are i/p of logic gate and Y is the o/p.

Operation:-

- (i) When the transistor operates in saturation region maximum current flow through the RC resistor. The o/p voltage $V_Y = V_{CE_{sat}}$

($V_{CEsat} = 0.2V$ for silicon and $0.1V$ for germanium)

(i) It is logic 0 level voltage when the transistor operate in cutoff. No current flow through RC and the o/p voltage $V_y = V_{CC} = 5V$

(ii) It is logic 1 level voltage

(i) When both i/p in logic zero transistor T_1 & T_2 operate in cutoff and the o/p is $+V_{CC}$ (logic 1)

(iii) When any one of the i/p is at logic 1 level the corresponding transistor operate in saturation region & the o/p is logic 0.

(iv) When both the i/p are at logic 1 level both the transistor operate in saturation & output is logic 0.

(v) Transistor Transistor Logic (TTL) with passive pullup $\Rightarrow$

(i) TTE passive pullup $V_{CC} = +5V$

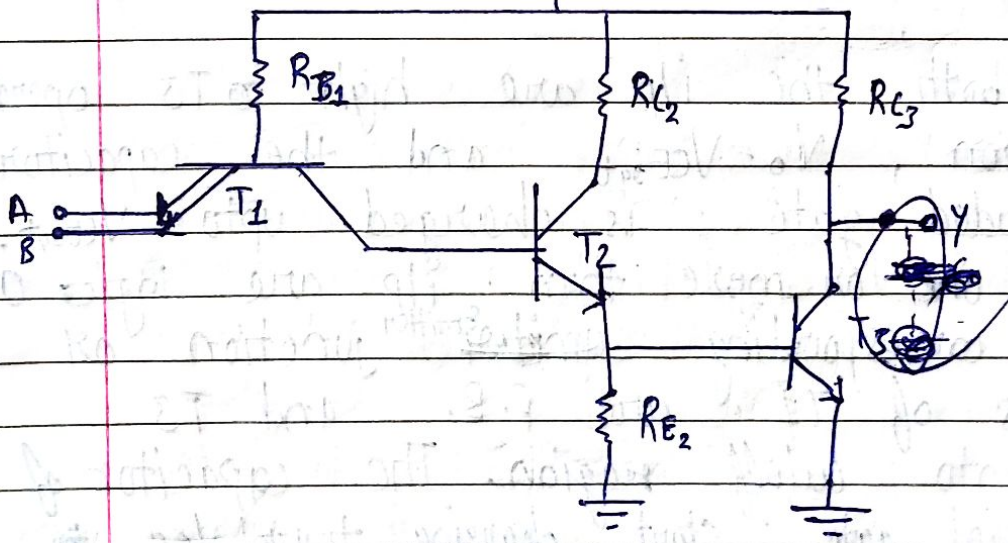


Fig. — Two input TTL NAND gate with passive pullup

Transistor Transistor Logic :-

POPU

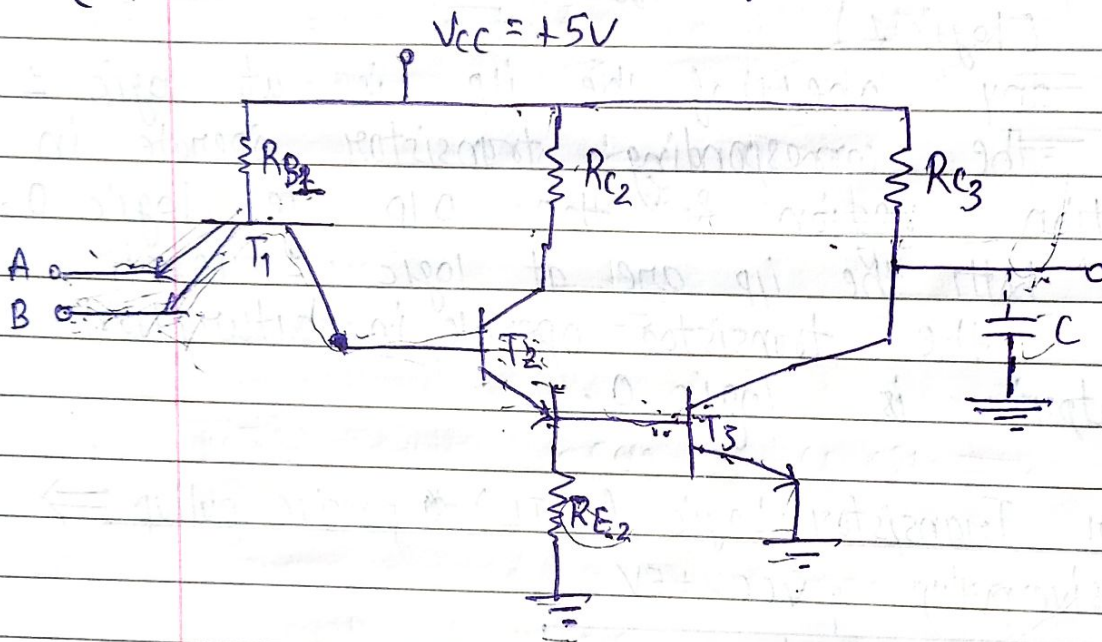
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A	B	Transistor T1		Transistor T2 & T3	Output
		Emitter Junction A	Emitter Junction B		
logic 0	logic 0	FB	FB	Cutoff	Logic 1
logic 0	logic 1	FB	RB	Cutoff	logic 1
logic 1	logic 0	RB	FB	Cutoff	logic 1
logic 1	logic 1	RB	RB	Saturation	logic 0

operation:-
 (i) logic 0
 (ii) logic 1 and logic 0
 (iii) logic 1 & logic 1

(A) TTL Passive Pull up :-



- (i) When both the i/p are high T_3 operates in saturation, $V_o = V_{CE_{sat}}$ and the capacitor of loaded gate is charged upto $V_{CE_{sat}}$.
- (ii) When one or more than i/p are logic 0 the corresponding emitter junction or junctions of T_1 are F.B. and T_3 goes into cutoff region. The capacitor of the loaded gate start charging toward V_{cc} through the resistor R_3 . The capacitor of the loaded gate is pulled toward V_{cc} through the passive component R_3 , Hence this circuit is known as "TTL with passive pullup".

(ii) TTL with totem pole $\Rightarrow$

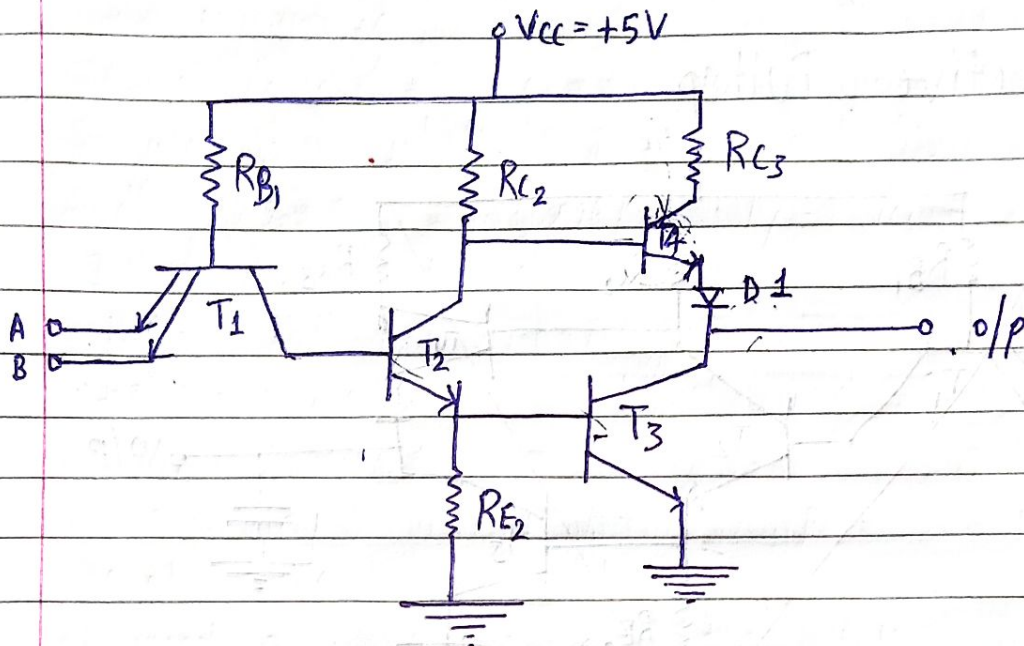


fig :- Two I/P TTL NAND Gate with totem pole

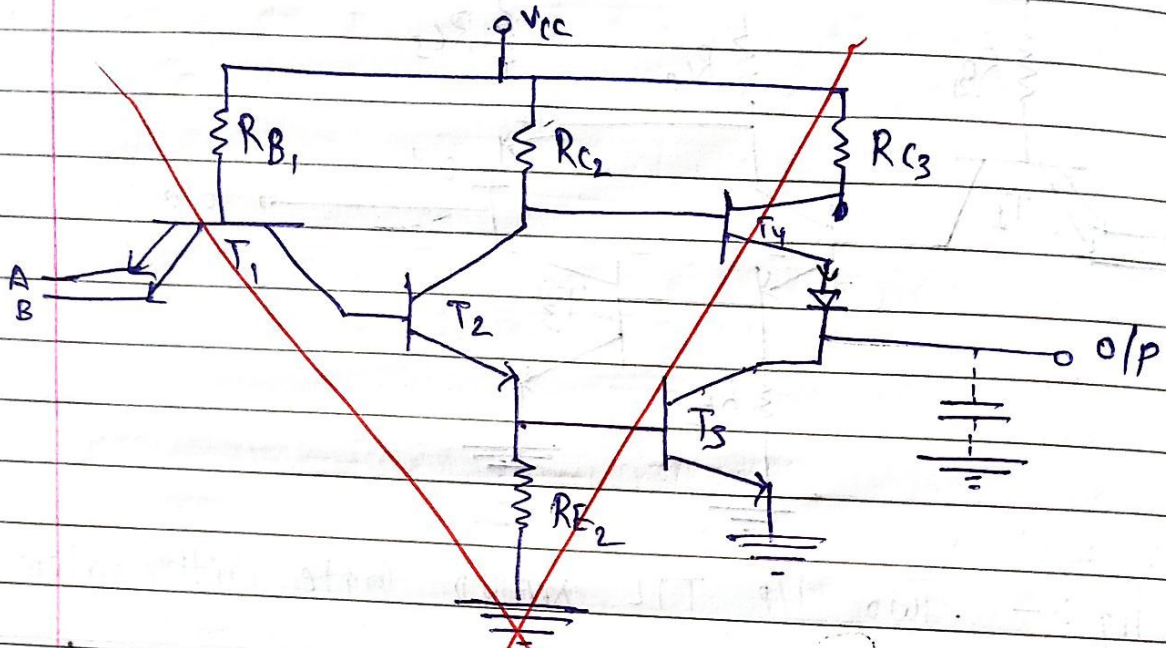
		Transistor 1		T2 & T3	T4	O/P
A	B	Junction emitter A	JEB	Transistor		
logic 0	logic 0	FB	FB	Cutoff	Saturation	logic 1
logic 0	logic 1	FB	RB	Cutoff	Saturation	logic 1
logic 1	logic 0	RB	FB	Cutoff	Saturation	logic 1
logic 1	logic 1	RB	RB	Saturation	Cutoff	logic 0

Operation :-

- (i) If all inputs are logic 0 then junction emitter A & B in forward bias. On logic 0 input T_1 is in cutoff that's why T_2 & T_3 is also in cutoff region and the full current voltage will flow in T_4 terminal then T_4 in Saturation region & output will logic 1.
- (ii) If any one input is logic 1 then T_1 , T_2 & T_3 in cutoff & T_4 is saturation region.
- (iii) If all inputs are logic 1 then Junctions in RB and Saturation region that's why T_4 will cutoff & o/p logic 0.

(ii)

Active Pullup



(iii) TTL with open collector $\Rightarrow$

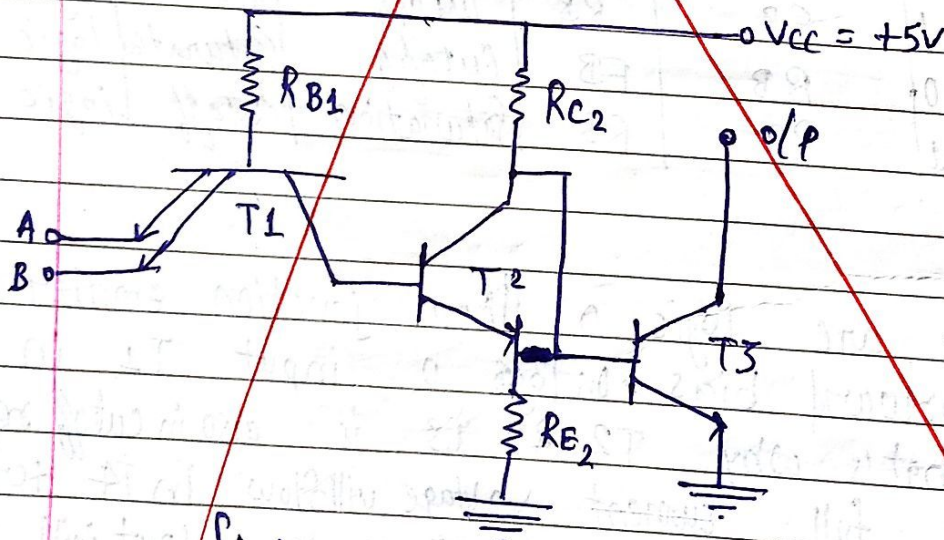


fig: 2 ilp TTL NAND gate with open collector

This is right... kindly ignore cross mark

THIS IS RIGHT.... kindly ignore cross mark

A	B	Transistor 1		Transistor T ₂	Transistor T ₃	o/p
		Emitter A	Emitter B			
logic 0	logic 0	FB	FB	Cutoff	Saturation	logic 1
logic 0	logic 1	FB	RB	Cutoff	Saturation	logic 1
logic 1	logic 0	RB	FB	Cutoff	Saturation	logic 1
logic 1	logic 1	RB	RB	Saturation	Cutoff	logic 0

Operation:-

1. If inputs are logic 0 then both emitter A & B will be in forward bias therefore T₂ in cutoff & T₃ in saturation region. Due to T₃ in saturation, output will logic 1.
2. If one input is logic 1 then one emitter will be in Reverse bias and other emitter in forward bias. Therefore T₂ in cutoff & T₃ in saturation region. Then output will logic 1.
3. If both inputs are logic 1 then both emitter A & B will be in reverse bias therefore T₂ in saturation & T₃ in cutoff. Due to T₃ in cutoff then output will logic 0.

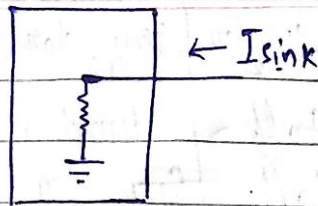
(iv) Tri-state TTL $\Rightarrow$ 1

A normal circuit has to a 2 output state low & high. If the o/p is not in the high state it is definitely in the low state. The tri-state TTL has 3 output state-high, low & high impedance.

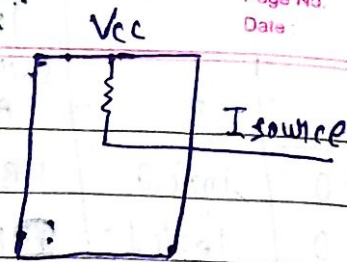
(iv) Tristate TTL:-

POPU

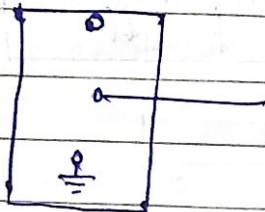
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(a) Low



(b) High



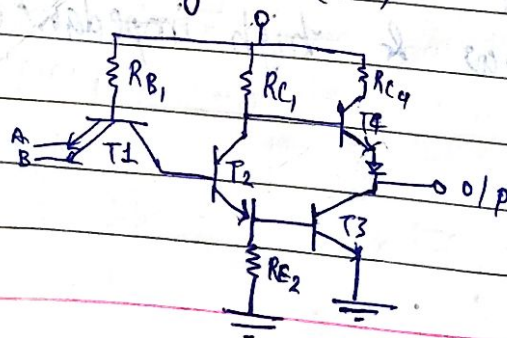
(c) High impedance

In TTL with totem pole output T_3 is on when the o/p is low and T_4 is on when the o/p is high. In High impedance state, both T_3 & T_4 in totem pole arrangement are turned off and as a result the o/p is open ~~and~~ or floating.

→ When the o/p is low the driver gate sink the load current as shown in figure (a).

→ When the o/p is high the driver gate supply the current to the load as shown in figure (b).

→ When the o/p is in high impedance state it acts as open or floating and there is no sink & source current as shown in figure (c).



use for amplifying or switching electronic signals

Page No. :
Date :
POPU

Mosfet $\Rightarrow$

(Metal oxide semiconductor field effect transistor)

MOSFET are very popular due to their low power dissipation & high density of fabrication. The logic families of MOSFET can be classified into three categories

- (i) NMOS
- (ii) PMOS
- (iii) CMOS

PMOS logic is slow as compare NMOS logic. Hence, it is not used in new design.

(i) NMOS: — MOSFETS are of two types: —
(a) Depletion (b) Enhancement types
NMOS families used only enhancement type mosfet.

(ii) PMOS: — PMOS are known as p-channel MOSFET.

(iii) CMOS: — CMOS family use n-channel & p-channel MOSFET. In CMOS, p-channel & n-channel mos devices are fabricated on the same chip which make its fabrication complicated but it reduces the packaging density & has small power consumption. Hence, CMOS is ideally suitable for battery operated system.

It allows high density of logic functions on a chip

CMOS inverter : — V_{CC}

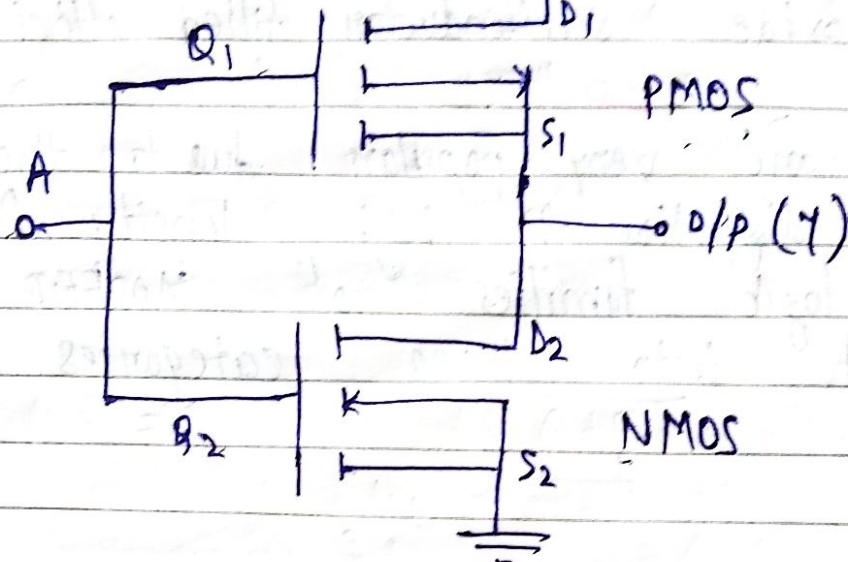
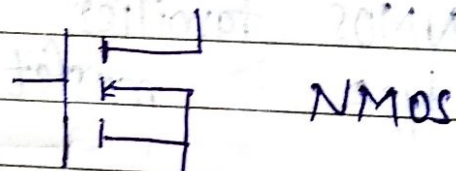
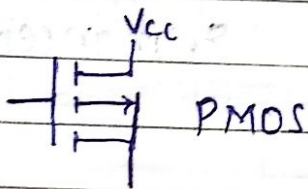


fig:- CMOS inverter

A	Q_1	Q_2	O/P
0	ON	OFF	1
1	OFF	ON	0

Note:-



$\left\{ \begin{array}{l} \text{PMOS} - \text{Series} \\ \updownarrow \\ \text{NMOS} - \text{Parallel} \end{array} \right\}$

PMOS $\rightarrow + \rightarrow$ Series
 NMOS $\rightarrow + \rightarrow$ parallel

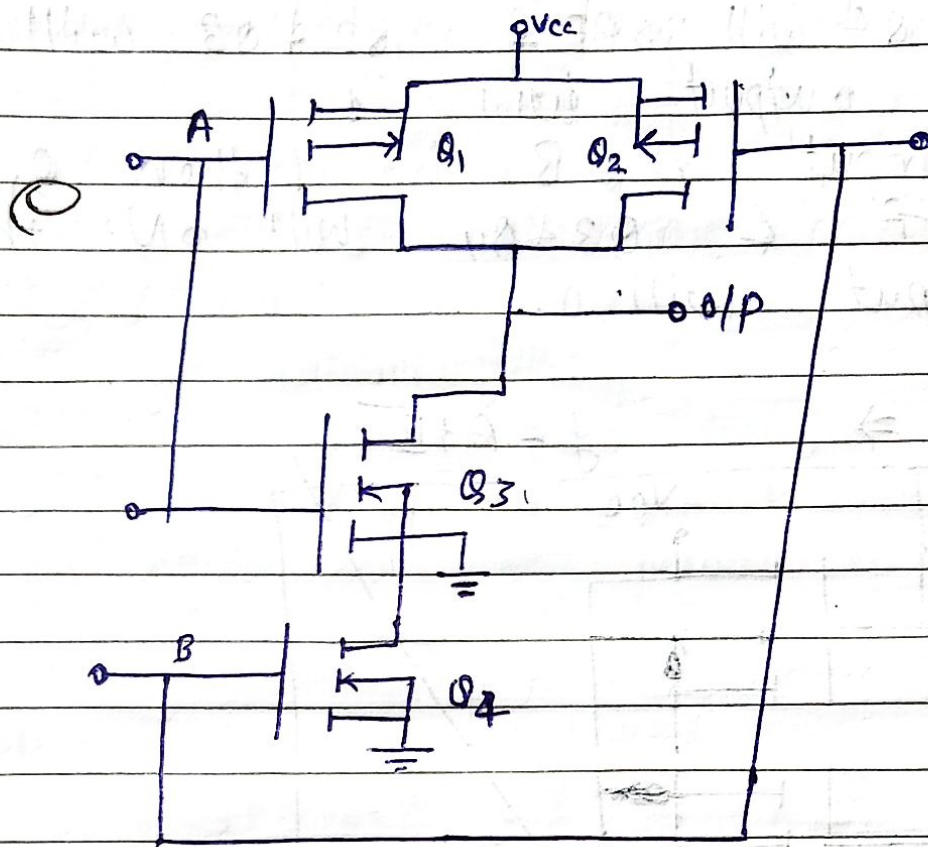
PMOS $\rightarrow (*) \rightarrow$ parallel
 NMOS $\rightarrow (*) \rightarrow$ series

PPP

(i)

NAND $\Rightarrow$

$$Y = \overline{AB}$$



A	B	Q ₁	Q ₂	Q ₃	Q ₄	O/P
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

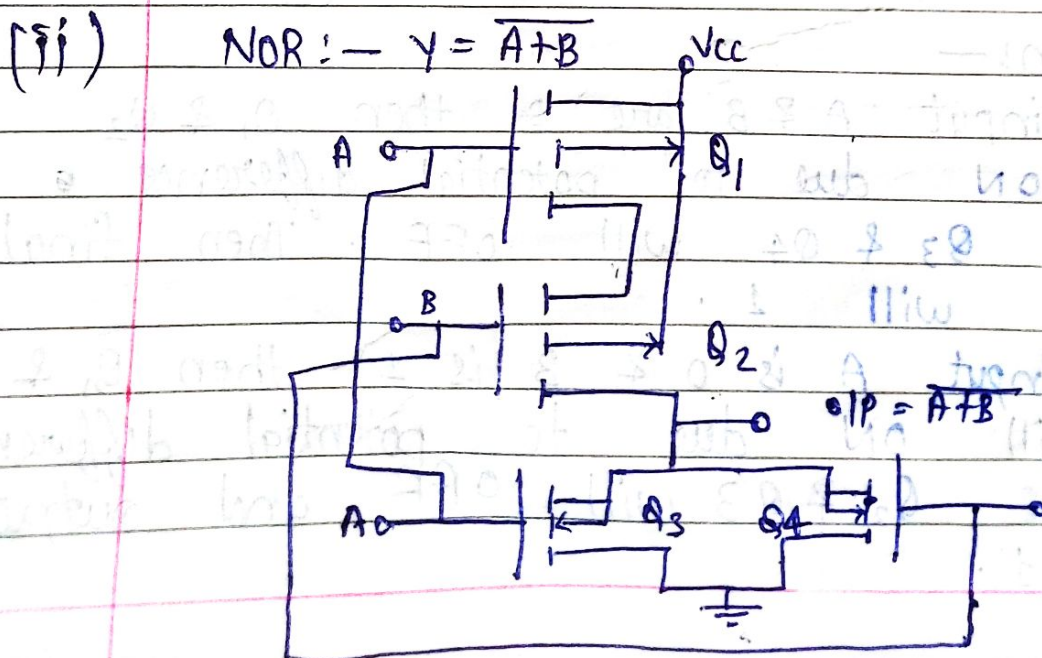
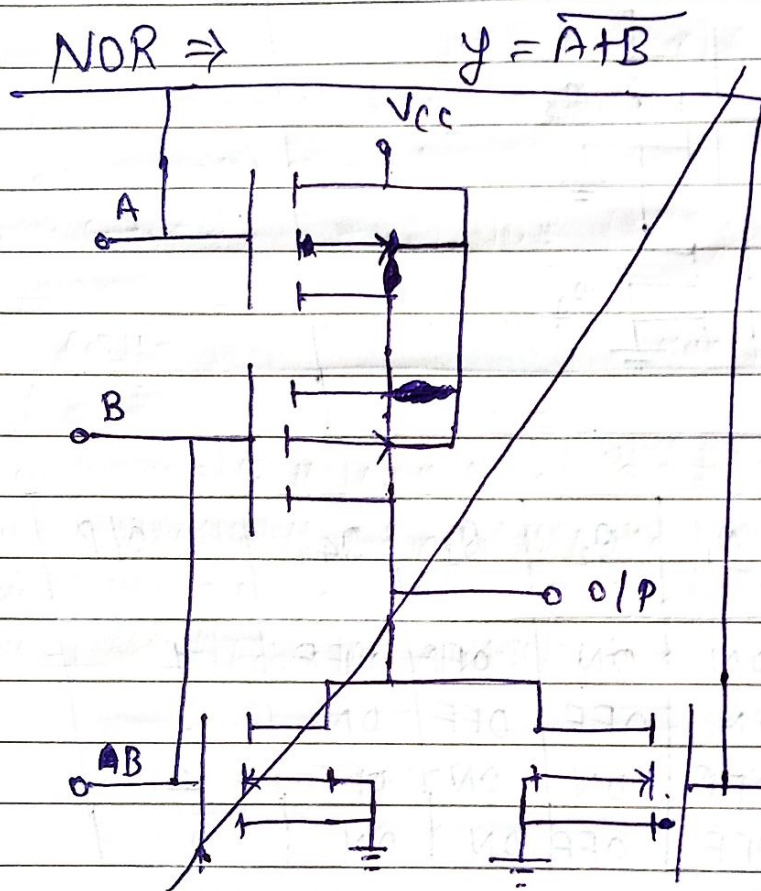
Operation:—

(i) If input A & B are 0 then Q₁ & Q₂ will ON due to potential difference & whereas Q₃ & Q₄ will OFF. Then final output will 1.

(ii) If input A is 0 & B is 1 then Q₁ & Q₄ will ON due to potential difference whereas Q₂ & Q₃ will OFF, and output will 1.

(iii) - If input A is 1 & B is 0 then Q_1 & Q_4 will off & Q_2 & Q_3 will ON then output will 1.

(iv) If input A & B is 1 then Q_1 & Q_2 will off & Q_3 & Q_4 will ON then output will 0.



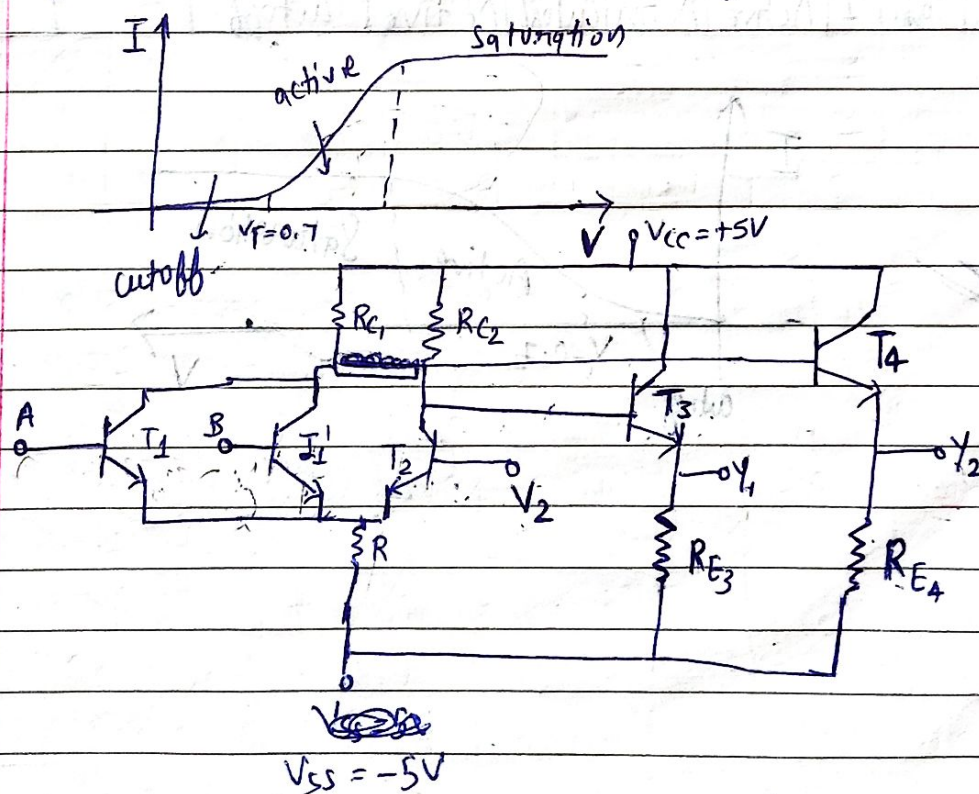
A	B	Q_1	Q_2	Q_3	Q_4	o/p
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	0
1	0	OFF	ON	ON	OFF	0
1	1	OFF	OFF	ON	ON	0

operation: — (i) (ii) (iii) (iv)

ECL (Emitter ~~coupled~~ coupled logic): —

A Emitter coupled logic (ECL) is faster than TTL family. The transistor of ~~an~~ ECL are operated in cutoff & active region. It never was in saturation region & there for this wrong time is eliminated. eliminated.

ECL family is an example of unsaturated logic family. The figure shown the circuit of emitter coupled logic OR/NOR gate

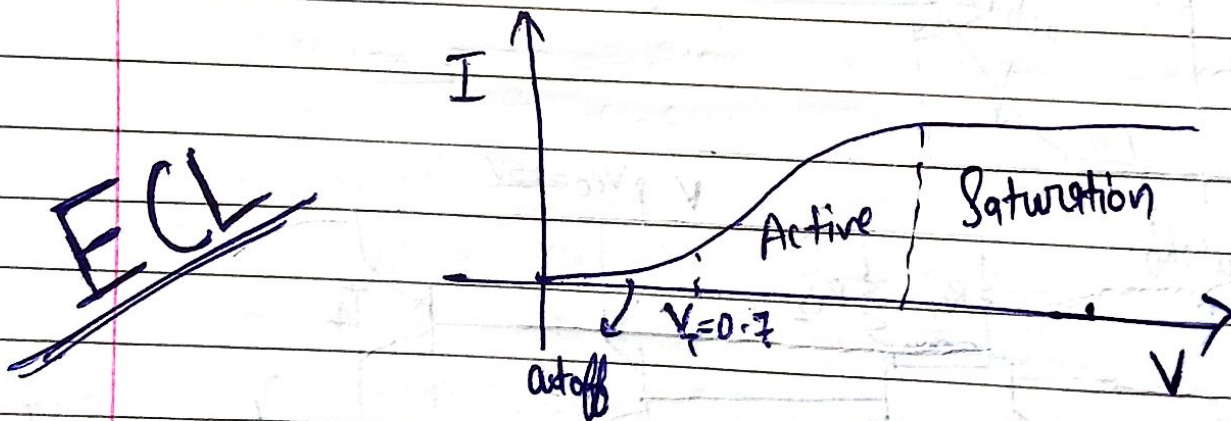


ECL OR/NOR gate

The circuit (ECL OR/NOR gate) consists of a difference amplifier and emitter followers. The emitter terminal of the 2 transistors are connected together. it is called as ECL.

The emitter followers are used at the o/p of difference amplifier to shift the DC level. The circuit has two o/p y_1 & y_2 which are complementary. y_1 correspond to OR logic & y_2 correspond to NOR logic.

Input		Input Transistor			Transistor		Output	
A	B	T_1	T_1'	T_2	T_3	T_4	y_1	y_2
logic 0	logic 0	Cutoff	Cutoff	Active	Cutoff	Active	0	1
logic 0	logic 1	Cutoff	Active	Cutoff	Active	Cutoff	1	0
logic 1	logic 0	Active	Cutoff	Cutoff	Active	Cutoff	1	0
logic 1	logic 1	Active	Active	Cutoff	Active	Cutoff	1	0

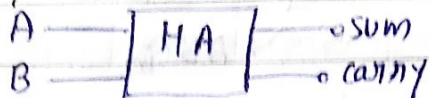


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Unit - 4

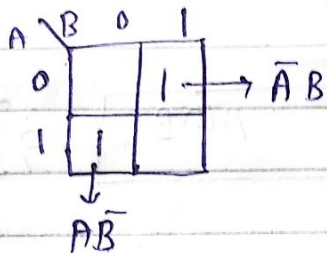
Adder: —

(i) Half adder: $\Rightarrow$



i/p		o/p	
A	B	sum	carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

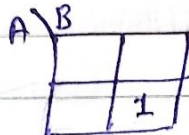
sum $\Rightarrow$



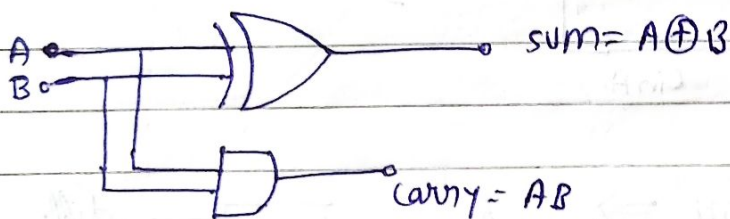
$$\text{sum} = \bar{A}B + A\bar{B}$$

$$\boxed{\text{sum} = A \oplus B}$$

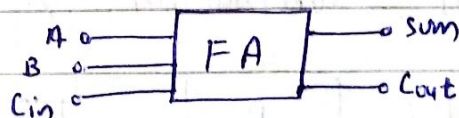
carry $\Rightarrow$



$$\boxed{\text{carry} = AB}$$



(ii) FULL ADDER: —



i/p			o/p	
A	B	Cin	sum	carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$A \oplus B = AB + \bar{A}\bar{B}$$

$$(\bar{A}B + A\bar{B}) \oplus C$$

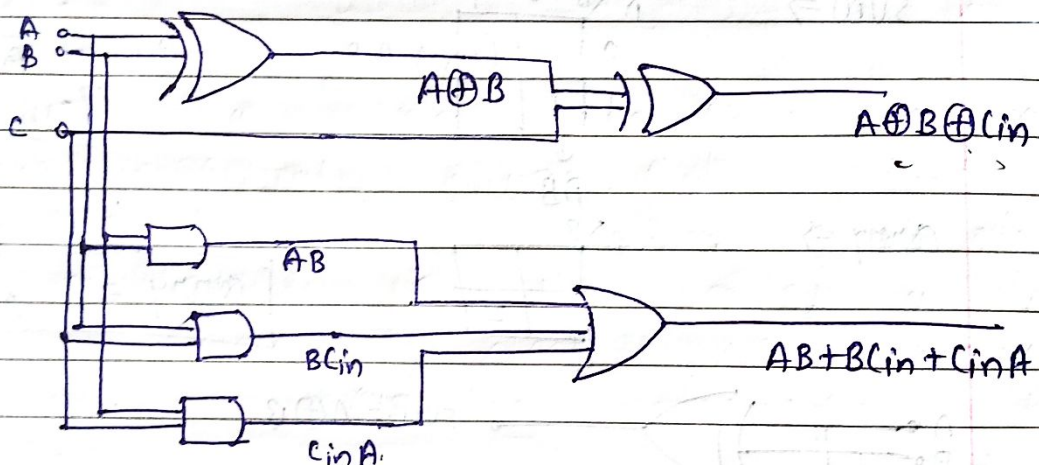
Sum $\Rightarrow$

	BCin			
	00	01	11	10
A				
0		1		1
1	1		1	

Labels: $\bar{A}\bar{B}C_{in}$ (00), $\bar{A}B\bar{C}_{in}$ (01), $AB\bar{C}_{in}$ (11), $A\bar{B}C_{in}$ (10)

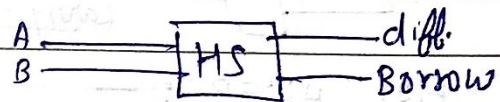
$$\begin{aligned} \text{Sum} &= \bar{A}\bar{B}C_{in} + \bar{A}B\bar{C}_{in} + AB\bar{C}_{in} + A\bar{B}C_{in} \\ &= \bar{A}(B \oplus C) + AB\bar{C}_{in} + A\bar{B}C_{in} \\ &= \bar{A}(B \oplus C_{in}) + A(B \oplus C_{in}) \\ \text{Sum} &= A \oplus B \oplus C_{in} \end{aligned}$$

carry:— $AB + BC_{in} + C_{in}A$



Subtractor:—

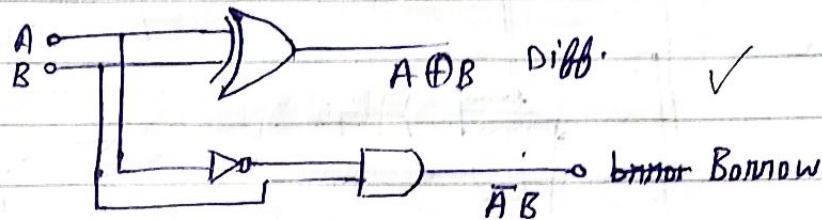
(i) Half Subtractor $\Rightarrow$



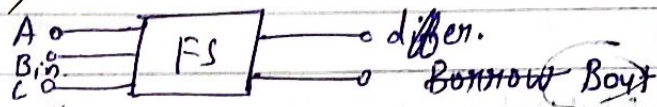
Ques 3
1/1

A	B	diff.	borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Sum diff. $\rightarrow \bar{A}B + A\bar{B} = A \oplus B$
 borrow $\rightarrow \bar{A}B$



(ii) Full subtractor $\Rightarrow$



A	I/P B _{in}	C	O/P Diff.	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

$$\begin{array}{r} 10^2 \\ -1 \\ \hline 9 \end{array} \quad \begin{array}{r} 1 \\ -0 \\ \hline 1 \end{array} \checkmark$$

Diff. =

A \ B C	00	01	10	11
0		1		1
1	1		1	

$$\bar{A}\bar{B}C + A\bar{B}\bar{C} + AB\bar{C} + \bar{A}B\bar{C}$$

$$\bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + B\bar{C})$$

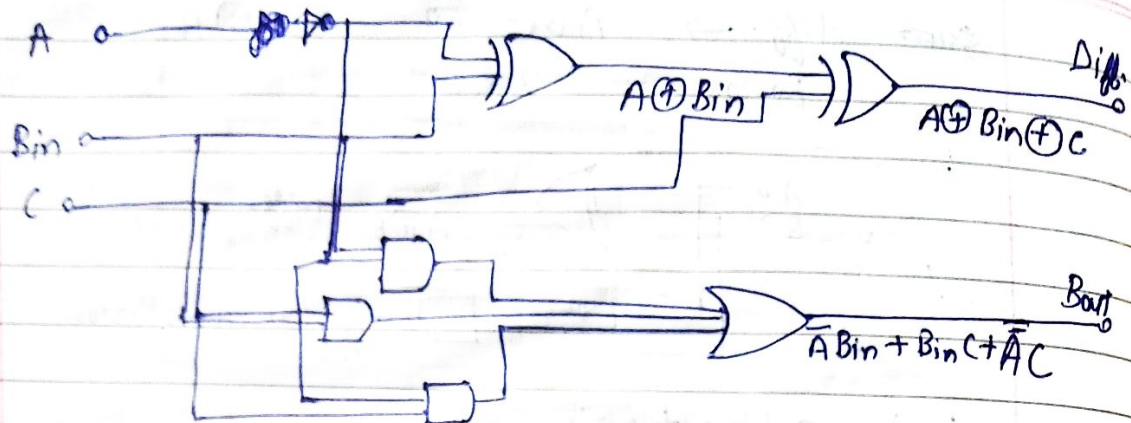
$$\bar{A}(B_{in} \oplus C) + A(B_{in} \odot C) = A \oplus B_{in} \oplus C$$

$$\text{Diff} = A \oplus B_{in} \oplus C$$

$$\text{Bout} = \bar{A}\bar{B}_{in}C + \bar{A}B_{in}\bar{C} + \bar{A}B_{in}C + AB_{in}C$$

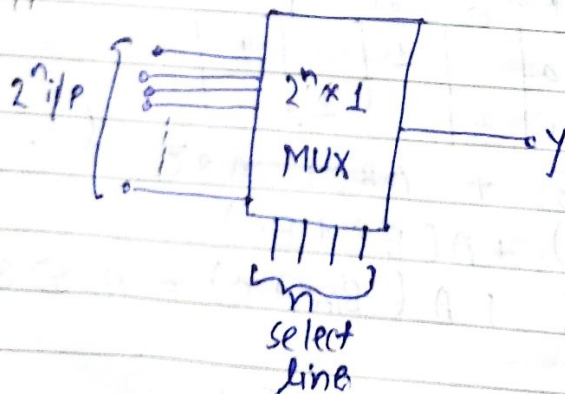
$$\bar{A}(B_{in} \oplus C) + B_{in}C(A + \bar{A})$$

$$= \bar{A}(B_{in} \oplus C) + B_{in}C = \bar{A}B_{in} + B_{in}C + \bar{C}\bar{A}$$



Multiplexer:- The term multiplex means many into one. Multiplexing is the process of transmitting over all single line.

- A digital multiplexer (MUX) is a combinational circuit that selects one digital information from several sources. And transmit the selected information on a single o/p line.
- A multiplexer is also called a data selector since it selects one of many inputs. And send the information to the o/p.



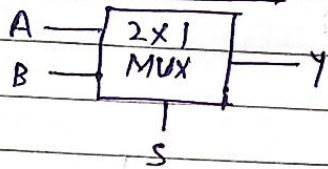
If i/p is 2^n then the select line will be n .

Type of MUX:-

(i) 2x1 MUX
 ↓
 i/p → 2
 select line → 1

(ii) 4x1 MUX (iii) 8x1 MUX (iv) 16x1 MUX
 ↓ ↓ ↓
 i/p → 4 i/p → 8 i/p → 16
 select line → 2 select line → 3 select line → 4

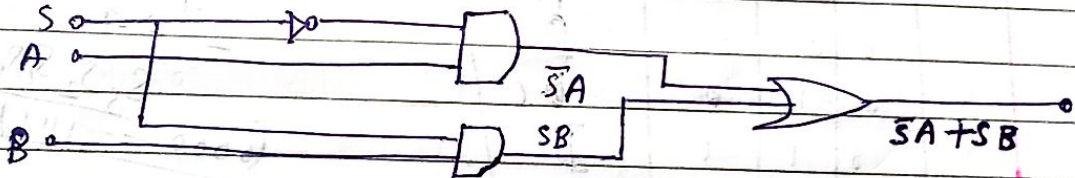
(i) 2x1 MUX :-



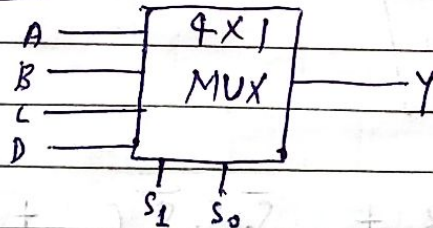
Truth Table - 2x1 MUX

i/p S	o/p Y
0	A
1	B

$$Y = \bar{S}A + SB$$



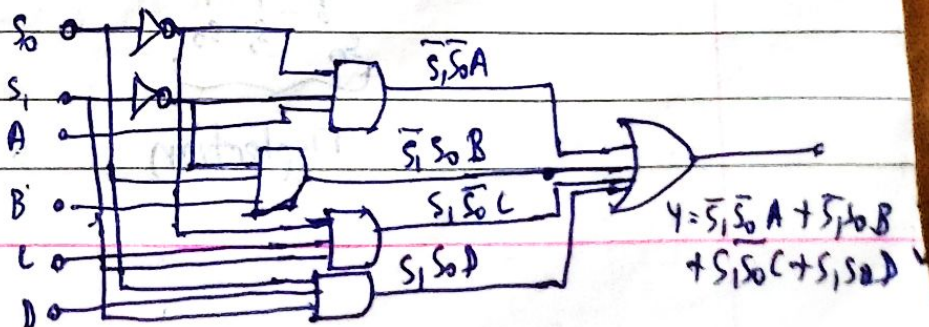
(ii) 4x1 MUX :-



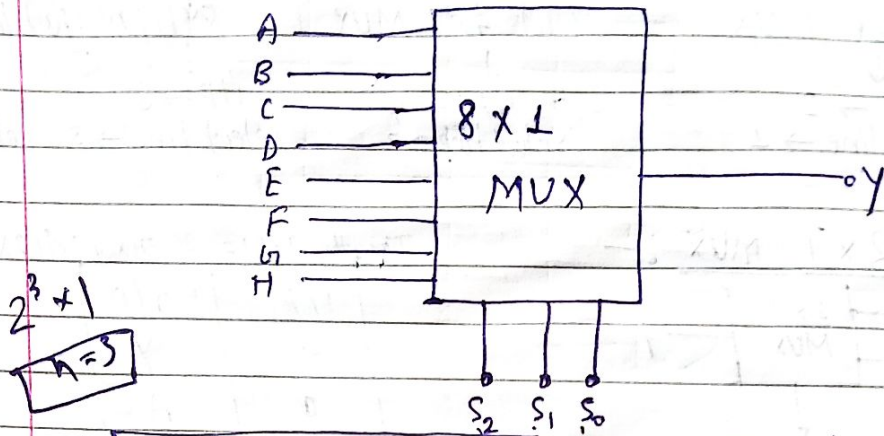
Truth table - 4x1 MUX

i/p		o/p
S ₁	S ₀	Y
0	0	I(0) = A
0	1	I(1) = B
1	0	I(2) = C
1	1	I(3) = D

$$Y = \bar{S}_1 \bar{S}_0 A + \bar{S}_1 S_0 B + S_1 \bar{S}_0 C + S_1 S_0 D$$



(5.) 8×1 MUX $\Rightarrow$



i/p			o/p
S_2	S_1	S_0	
0	0	0	A
0	0	1	B
0	1	0	C
0	1	1	D
1	0	0	E
1	0	1	F
1	1	0	G
1	1	1	H

16×1

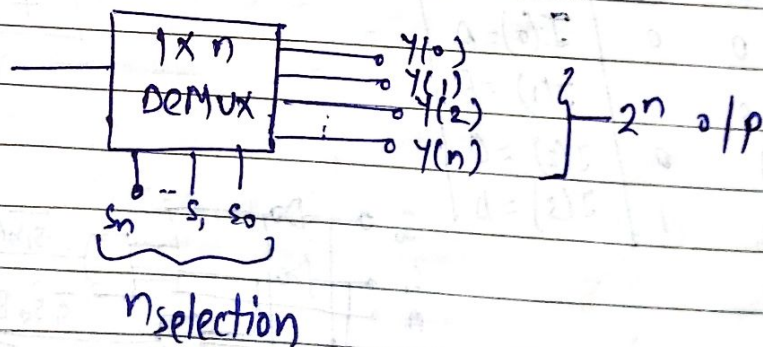


$2^4 \Rightarrow 4$

$$\begin{array}{r} S_3 S_2 S_1 S_0 \\ 6000 \quad \underline{\quad 1111 \quad} \end{array}$$

$$Y = \bar{S}_2 \bar{S}_1 \bar{S}_0 A + \bar{S}_2 \bar{S}_1 S_0 B + \bar{S}_2 S_1 \bar{S}_0 C + \bar{S}_2 S_1 S_0 D + S_2 \bar{S}_1 \bar{S}_0 E + S_2 \bar{S}_1 S_0 F + S_2 S_1 \bar{S}_0 G + S_2 S_1 S_0 H$$

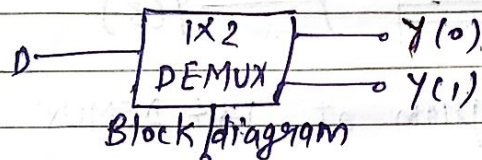
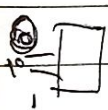
Demultiplexer: —



→ Demultiplexer is the process of taking information from the i/p & transmitting it to two or more o/p.

A demultiplexer is a logic ckt that receives information on a single i/p & transmit the same information over one of several (2^n) o/p.

* 1x2 DEMUX:—



Block diagram

o/p equations

$$Y(0) = \bar{S} D$$

$$Y(1) = S D$$

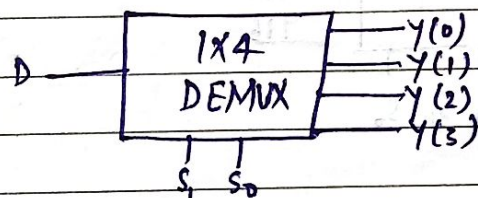
truth table

i/p	S	Y(1)	Y(0)
0	0	0	D
	1	D	0

circuit diagram



* 1x4 DEMUX:—



o/p

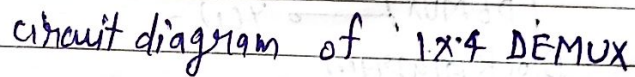
$$Y(0) = \bar{S}_1 \bar{S}_0 D$$

$$Y(1) = \bar{S}_1 S_0 D$$

$$Y(2) = S_1 \bar{S}_0 D$$

$$Y(3) = S_1 S_0 D$$

i/p	Select line	Y(3)	Y(2)	Y(1)	Y(0)
	S ₁ S ₀				
0	0 0	0	0	0	D
	0 1	0	0	D	0
	1 0	0	D	0	0
	1 1	D	0	0	0



1x16

DEMUX

S_3 S_2 S_1 S_0

$$\begin{array}{r} 1010101 \\ + 111111 \\ \hline 1100011 \\ \hline \end{array}$$

Truth table: —

[illegible]



$S_3 S_2 S_1 S_0$ ✓

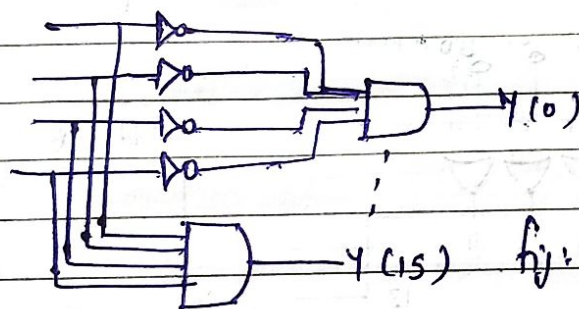


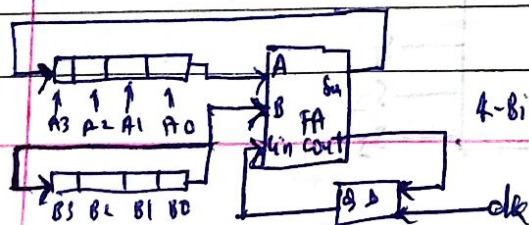
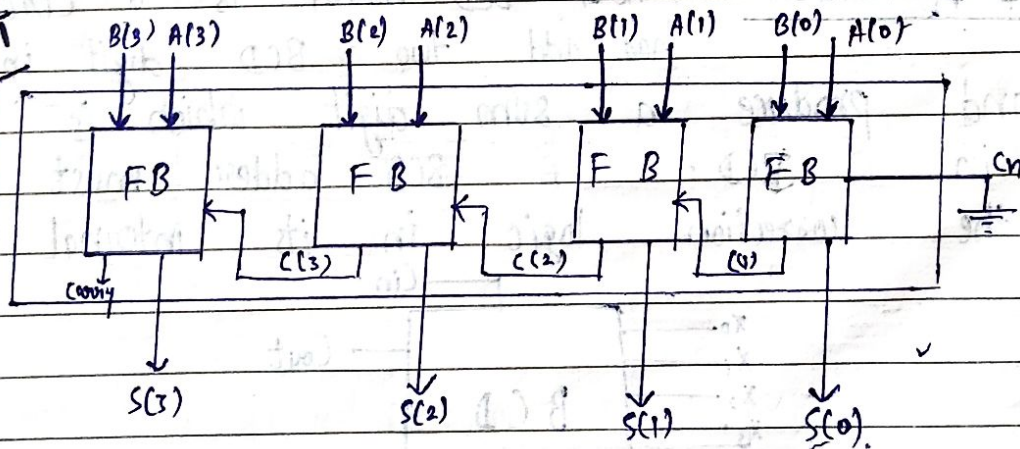
fig: circuit diagram of 1x16 DEMUX. ✓

4-BITS ADDER ⇒

Carry ripple :-

$$\begin{array}{r} 1010 \\ + 1111 \\ \hline 1001 \end{array}$$

$$\begin{array}{r} 110 \\ \text{eg - } A - 1010 \text{ } A_4 \\ B - 1111 \text{ } B_4 \\ \hline 101001 \end{array}$$



4-bit serial adder using shift registers

011013

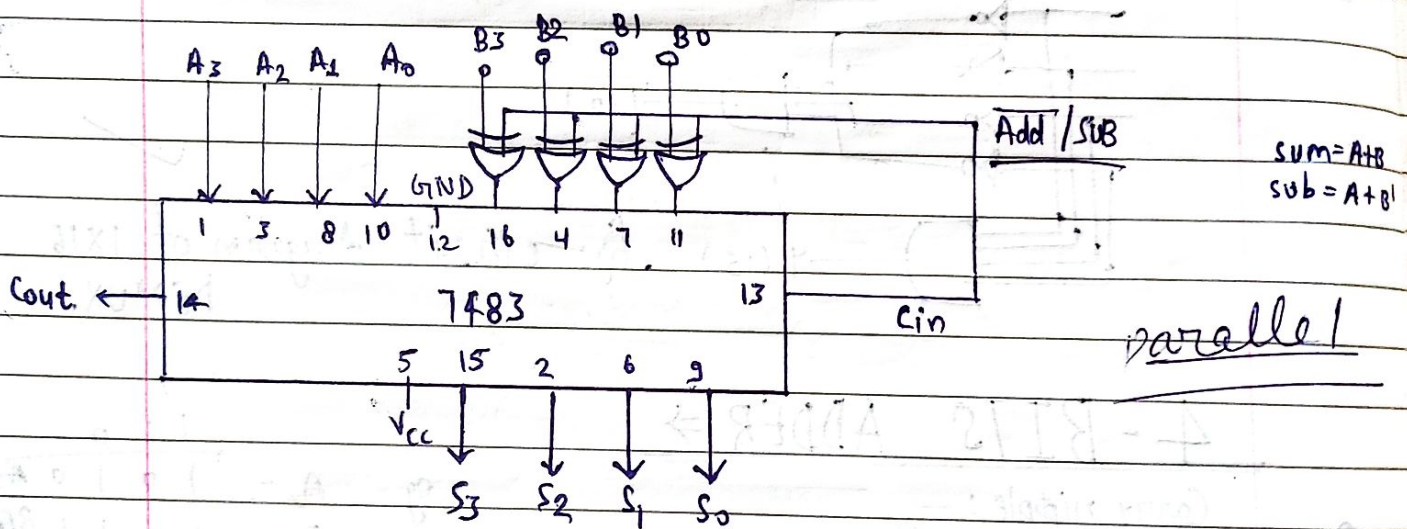
Page No.
Date

7F	0	0
0	0	0
POP	0	1
1	1	1
1	1	0

parallel 4-BIT Adder / Subtractor $\Rightarrow$

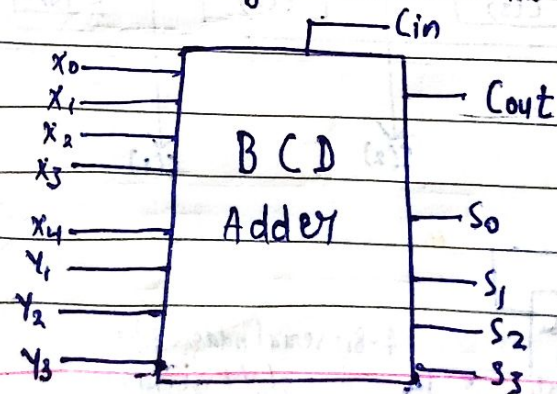
$\rightarrow$ 1001 - 1000 using 1's

$$\begin{array}{r}
 1001 \\
 1000 \\
 \hline
 0001 \\
 \textcircled{1} 0001 \quad \text{Carry} \leftarrow \\
 \hline
 0001 \\
 + 1 \\
 \hline
 0001
 \end{array}$$



* BCD Adder $\Rightarrow$

The BCD Adder is a circuit that add two BCD digit in parallel and produce a sum digit which is also in BCD. A BCD adder must include the correction logic in its internal construction.



A BCD adder circuit must be able to do following:

- (i) ~~Add~~ Add two 4-bit BCD number using binary addition.
- (ii) If the ~~for~~ 4-bit sum is equal or less than 9 the sum is proper BCD form & no correction is needed.
- (iii) If the 4-bit sum is greater than 9 or if the carry is generated from the sum the sum is not in BCD form then a digital 6 (0110) should be added through the sum to produce the BCD result.
The carry may be produced due to this addition and it is added next decimal position.

Decimal No.	Uncorrected BCD sum					Corrected BCD sum				
	C ₃	S ₃	S ₂	S ₁	S ₀	Carry	S ₃	S ₂	S ₁	S ₀
0		0	0	0	0		0	0	0	0
1		0	0	0	1		0	0	0	1
2		0	0	1	0		0	0	1	0
3		0	0	1	1		0	0	1	1
4		0	1	0	0		0	1	0	0
5		0	1	0	1		0	1	0	1
6		0	1	1	0		0	1	1	0
7		0	1	1	1		0	1	1	1
8		1	0	0	0		1	0	0	0
9		1	0	0	1		1	0	0	1
10		1	0	1	0	1	0	0	0	0
11		1	0	1	1	1	0	0	0	1
12		1	1	0	0	1	0	0	1	0
13		1	1	0	1	1	0	0	1	1
14		1	1	1	0	1	0	1	0	0

NO correction Required

BCD 0 → 2V
② ↑ 10
+ 6
16 ✓

2 → 16

Correction Required

15	1	1	1	1	1	0	1	0	1
16	1	0	0	0	0	1	0	1	0
17	1	0	0	0	1	1	0	1	1
18	1	0	0	1	0	1	1	0	0
19	1	0	0	1	1	1	0	0	1

4 Variable ✓

$S_3 S_2$ \ $S_1 S_0$	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

Using K-Map

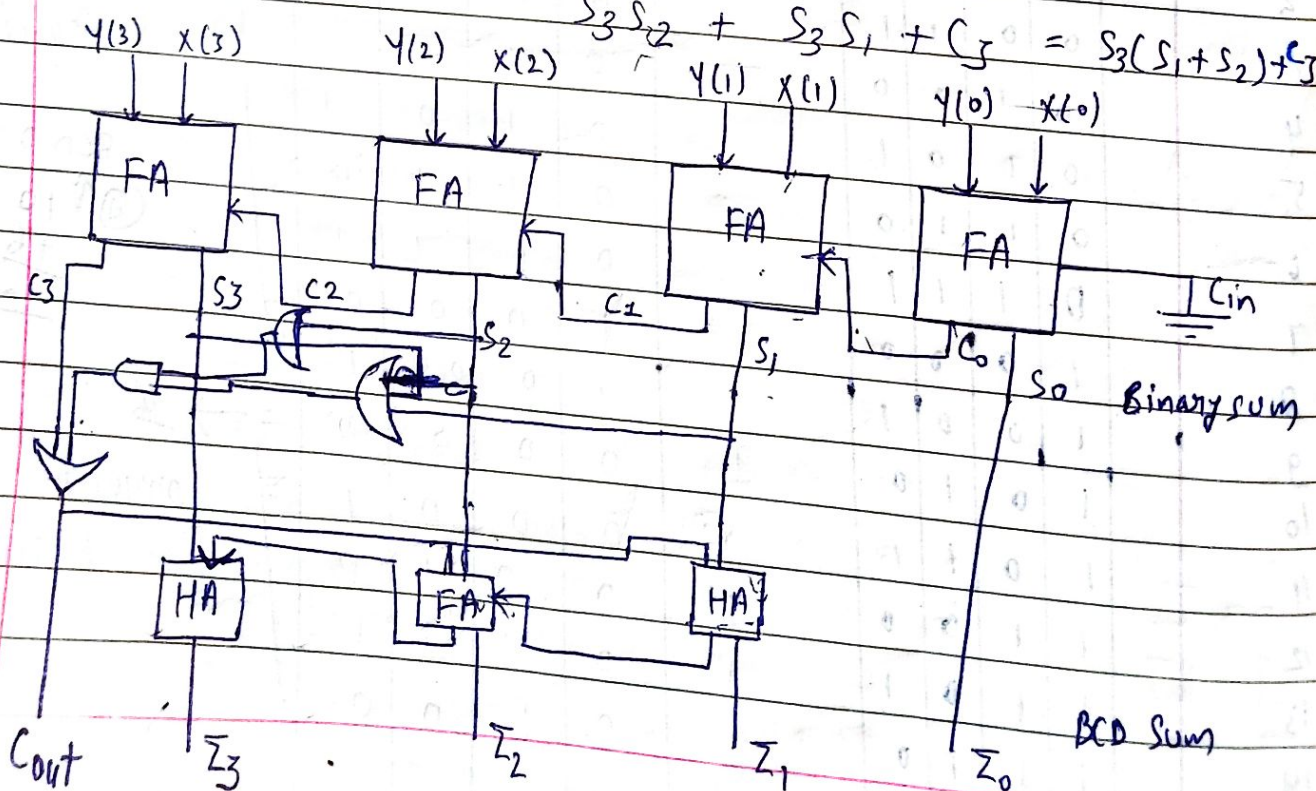
① → $\bar{S}_0 S_3 S_2$ ✓

② → $S_3 S_1$ ✓

$S_3 S_2 \bar{S}_0 + S_3 S_1 + C_3$

we don't consider complement so
new update eqn is

$S_3 S_2 + S_3 S_1 + C_3 = S_3(S_2 + S_1) + C_3$ ✓

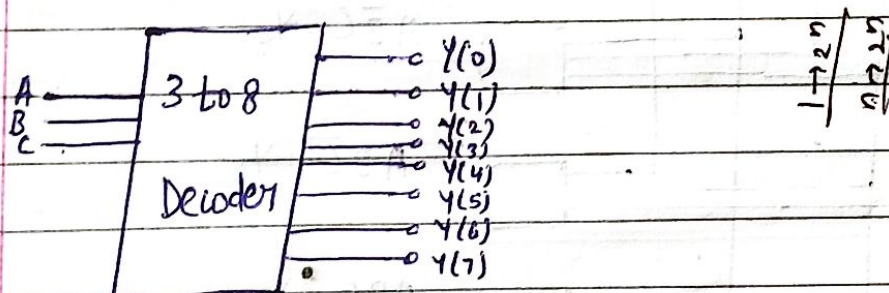


Encoder & Decoder $\Rightarrow$

Decoder:— Decoder is similar to Demultiplexer but ~~with~~ without any data input.

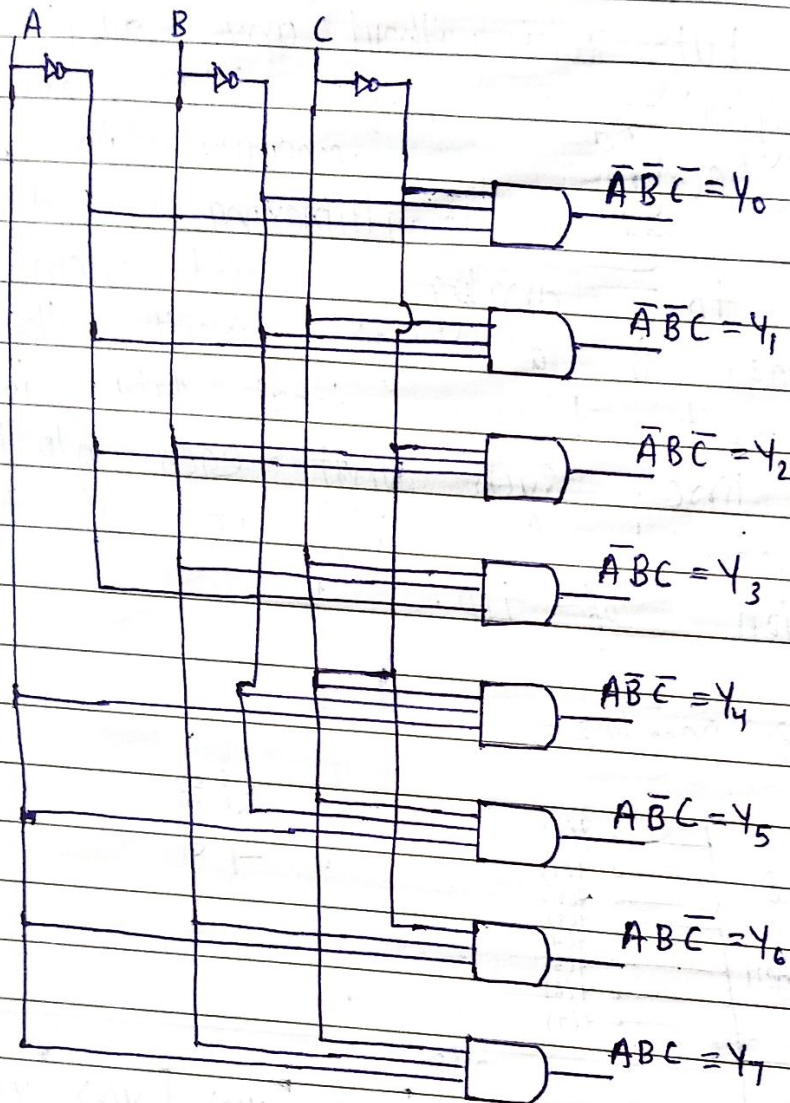
Most digital system require the decoding of data. Decoding is necessary in application such as data demultiplexing, digital display, digital to analog and memory addressing. A decoder is a logic circuit that converts ~~an~~ n -bit binary input data into 2^n output line. Such that each o/p line will be activated for only one of the possible combination of i/p.

(i) 3 to 8 Decoder $\Rightarrow$

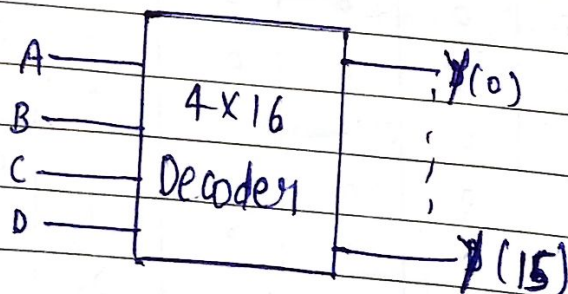


I/p			O/p							
A	B	C	Y(0)	Y(1)	Y(2)	Y(3)	Y(4)	Y(5)	Y(6)	Y(7)
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

$$\begin{aligned}
 Y(0) &= \bar{A}\bar{B}\bar{C}, & Y(1) &= \bar{A}\bar{B}C, & Y(2) &= \bar{A}B\bar{C} \\
 Y(3) &= \bar{A}BC, & Y(4) &= A\bar{B}\bar{C}, & Y(5) &= A\bar{B}C \\
 Y(6) &= AB\bar{C}, & Y(7) &= ABC
 \end{aligned}$$



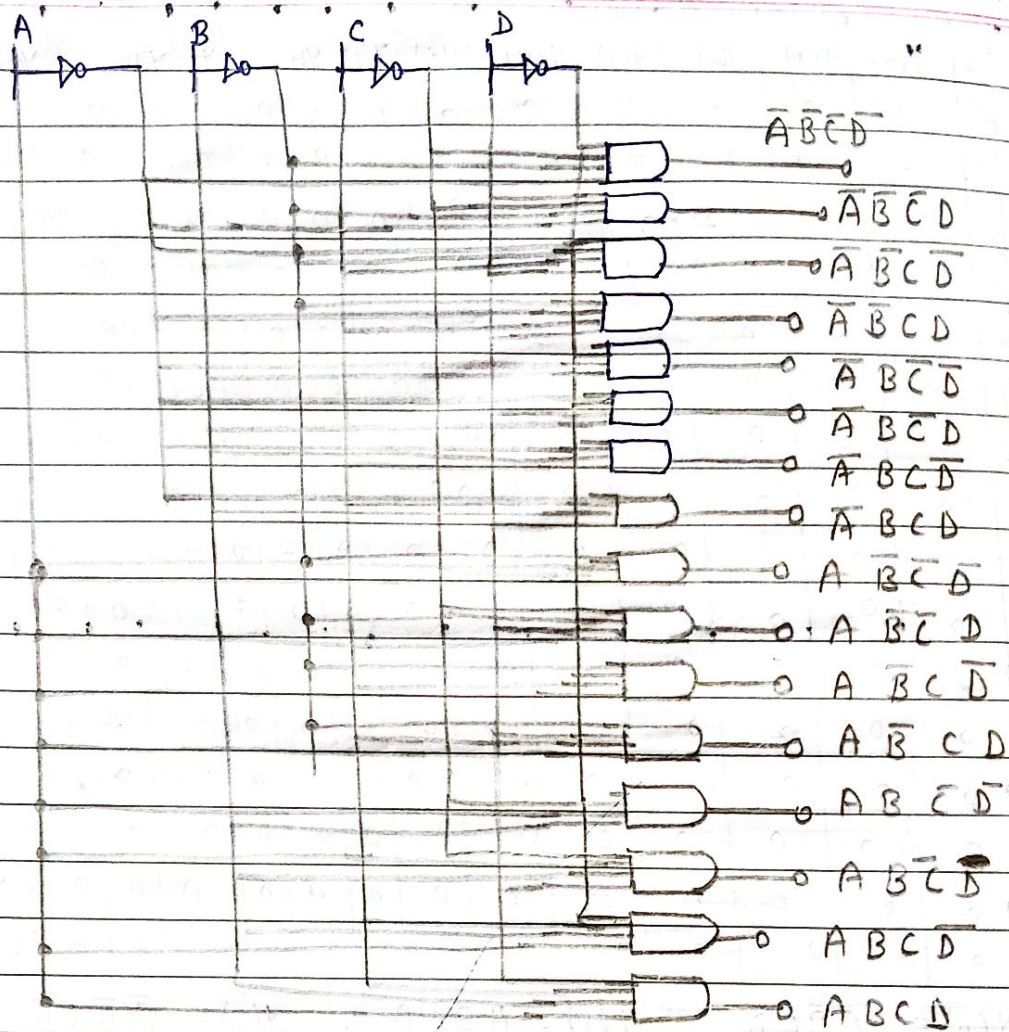
(ii) 4 x 16 Decoder $\Rightarrow$



(a) On Active Low $\Rightarrow$

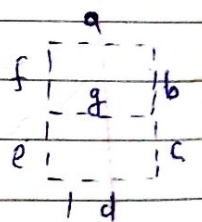
A	B	C	D	$\gamma(0)$	$\gamma(1)$	$\gamma(2)$	$\gamma(3)$	$\gamma(4)$	$\gamma(5)$	$\gamma(6)$	$\gamma(7)$	$\gamma(8)$	$\gamma(9)$	$\gamma(10)$	$\gamma(11)$	$\gamma(12)$	$\gamma(13)$	$\gamma(14)$	$\gamma(15)$
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

$$\begin{aligned}
 \gamma(0) &= \bar{A}\bar{B}\bar{C}\bar{D}, & \gamma(1) &= \bar{A}\bar{B}\bar{C}D, & \gamma(2) &= \bar{A}\bar{B}C\bar{D}, & \gamma(3) &= \bar{A}\bar{B}CD \\
 \gamma(4) &= \bar{A}B\bar{C}\bar{D}, & \gamma(5) &= \bar{A}B\bar{C}D, & \gamma(6) &= \bar{A}BC\bar{D}, & \gamma(7) &= \bar{A}BCD \\
 \gamma(8) &= A\bar{B}\bar{C}\bar{D}, & \gamma(9) &= A\bar{B}\bar{C}D, & \gamma(10) &= A\bar{B}C\bar{D} \\
 \gamma(11) &= A\bar{B}CD, & \gamma(12) &= AB\bar{C}\bar{D} \\
 \gamma(13) &= AB\bar{C}D \\
 \gamma(14) &= ABC\bar{D} \\
 \gamma(15) &= ABCD
 \end{aligned}$$



BCD to 7 segment $\Rightarrow$

BCD				7 seg						
A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	1	1	1	1	1	1	0
0	0	0	1	0	1	1	0	0	0	0
0	0	1	0	1	1	0	1	1	0	1
0	0	1	1	1	1	1	1	0	0	1
0	1	0	0	0	1	1	0	0	1	1
0	1	0	1	1	0	1	1	0	1	1
0	1	1	0	1	0	1	1	1	1	1
0	1	1	1	1	1	1	0	0	0	0
1	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	1	1	1	0	1	1



(i) $a \Rightarrow$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	d	d	d	d
10	1	1	1	1

Groupings: (1) covers all 1s in the first two columns (00, 01). (2) covers all 1s in the last two columns (11, 10). (3) covers all 1s in the first two rows (00, 01). (4) covers all 1s in the first two columns (00, 01).

- ① $\rightarrow \overline{A}\overline{D}$
 ② $\rightarrow \overline{B}C$
 ③ $\rightarrow BD$
 ④ $\rightarrow \overline{B}\overline{D}$

$$a = \overline{A}\overline{D} + \overline{B}C + BD + \overline{B}\overline{D}$$

$$a = \overline{D}(A + \overline{A}\overline{B}) + \overline{B}C + BD$$

$$a = \overline{D}((A + \overline{A})(A + \overline{B})) + \overline{B}C + BD$$

$$a = \overline{D}(A + \overline{B}) + \overline{B}C + BD$$

$$a = \overline{B}C + BD + \overline{B}\overline{D} + \overline{A}\overline{D}$$

$$a = \overline{A}\overline{D} + \overline{B}C + \overline{B}\overline{D} \checkmark$$

(ii)

For $b \Rightarrow$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	d	d	d	d
10	1	1	1	1

Groupings: (1) covers all 1s in the first two columns (00, 01). (2) covers all 1s in the last two columns (11, 10). (3) covers all 1s in the first two rows (00, 01). (4) covers all 1s in the first two columns (00, 01).

① $\rightarrow \overline{A}\overline{D}$ ② $\rightarrow \overline{B}\overline{D}$ ③ $\rightarrow \overline{B}C$ ④ $\rightarrow \overline{B}\overline{C}$

$$b = \overline{A}\overline{D} + \overline{B}\overline{D} + \overline{B}(C + \overline{C}) // \overline{B}(\overline{D} + C) + \overline{B}\overline{C}$$

$$b = \overline{A}\overline{D} + \overline{B}\overline{D} + \overline{B}(C + \overline{C}) // \overline{B}\overline{D}(\overline{D} + C) + \overline{B}C$$

$$b = \overline{A}\overline{D} + \overline{B}(\overline{D} + C) // \overline{B}(\overline{D} + C)$$

(iii)

for $c \Rightarrow$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	d	d	d	d
10	1	1	1	1

Groupings: (1) covers all 1s in the first two columns (00, 01). (2) covers all 1s in the last two columns (11, 10). (3) covers all 1s in the first two rows (00, 01). (4) covers all 1s in the first two columns (00, 01).

① $= \overline{B}\overline{D}$

② $= \overline{B}C$ ③ $= \overline{B}\overline{D}$

$$C = B\bar{D} + \bar{B}\bar{C} + \bar{B}D$$

$$C = B \oplus D + \bar{B}\bar{C}$$

④ For $d \Rightarrow$

AB \ C	00	01	11	10
00	1 ⁰	1	1 ³	1 ²
01		1 ⁵		1 ⁶
11	d ¹²	d ¹³	d ¹⁵	d ¹⁴
10	1 ⁸	1 ⁹	d ¹¹	d ¹⁰

② points to cell (01, 00) and (01, 01)
⑤ points to cell (11, 00) and (11, 01)
③ points to cell (10, 00) and (10, 01)
④ points to cell (01, 11) and (11, 11)
① points to cell (11, 10) and (10, 10)

① $\rightarrow A\bar{D}$ ② $\rightarrow \bar{B}\bar{D}$ ③ $\rightarrow \bar{B}\bar{C}$ ④ $\rightarrow \bar{B}\bar{C}\bar{D}$ ⑤ $\rightarrow B\bar{C}\bar{D}$

$$d = \bar{B}\bar{D}(1+1) + \bar{B}\bar{C} + B\bar{C}\bar{D} + A\bar{D}$$

$$d = \bar{B}\bar{D} + \bar{B}\bar{C} + B\bar{C}\bar{D} + A\bar{D}$$

⑤ For $e \Rightarrow$

AB \ C	00	01	11	10
00	1 ⁰	1	1 ³	1 ²
01		1 ⁵		1 ⁶
11	d ¹²	d ¹³	d ¹⁵	d ¹⁴
10	1 ⁸	1 ⁹	d ¹¹	d ¹⁰

① points to cell (00, 00) and (00, 01)
② points to cell (01, 00) and (01, 01)

① $\rightarrow \bar{B}\bar{D}$

② $\rightarrow \bar{B}\bar{C}\bar{D}$

$$e = \bar{B}\bar{D} + \bar{B}\bar{C}\bar{D}$$

$$e = \bar{B}\bar{D}(1+C)$$

$$e = \bar{B}\bar{D}$$

⑥ For $f \Rightarrow$

AB \ CD	00	01	11	10
00	1	0	1	3
01	1	1	5	7
11	d	d	d	d
10	1	1	d	d

① $\rightarrow A\bar{D}$ ② $\rightarrow \bar{B}\bar{C}\bar{D}$ ③ $\rightarrow B\bar{D}$ ④ $\rightarrow B\bar{C}$

$$f = \bar{B}\bar{C}\bar{D} + B\bar{D} + B\bar{C} + A\bar{D}$$

$$f = \bar{D}(B + \bar{C}) + B\bar{C} + A\bar{D}$$

⑦ For $g \Rightarrow$

AB \ CD	00	01	11	10
00	0	1	1	3
01	1	1	5	7
11	d	d	d	d
10	1	1	d	d

① $\rightarrow A\bar{D}$ ② $\rightarrow B\bar{C}$ ③ $\rightarrow \bar{B}\bar{C}\bar{D}$ ④ $\rightarrow \bar{B}\bar{C}$

$$g = A\bar{D} + \bar{B}\bar{C}\bar{D} + \bar{B}\bar{C} + B\bar{C}$$

$$g = A\bar{D} + \bar{B}\bar{C}(1 + \bar{D}) + B\bar{C}$$

$$g = A\bar{D} + \bar{B}\bar{C} + B\bar{C}$$

$$g = A\bar{D} + B\oplus C$$



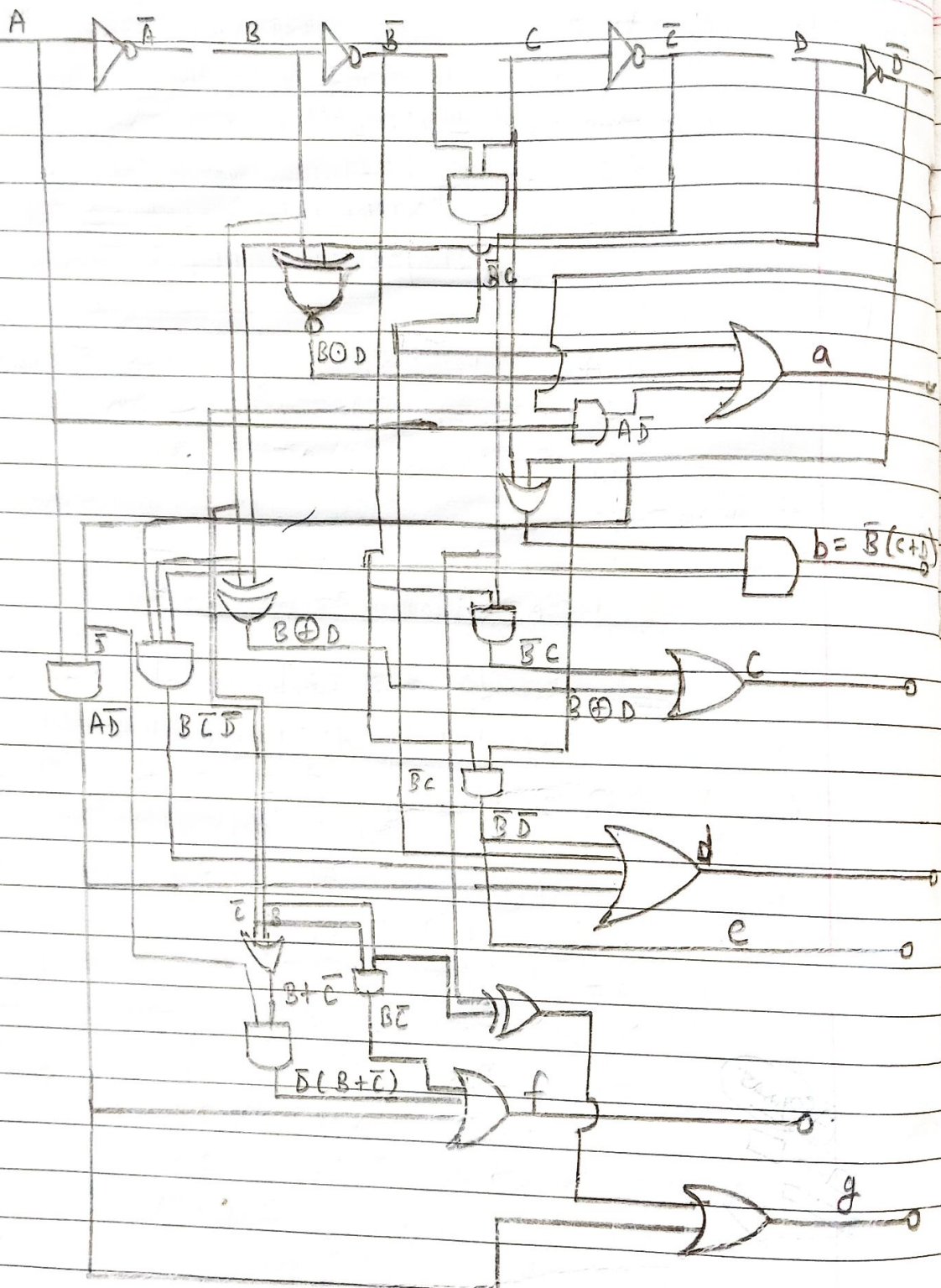


fig: - BCD to 7 segment

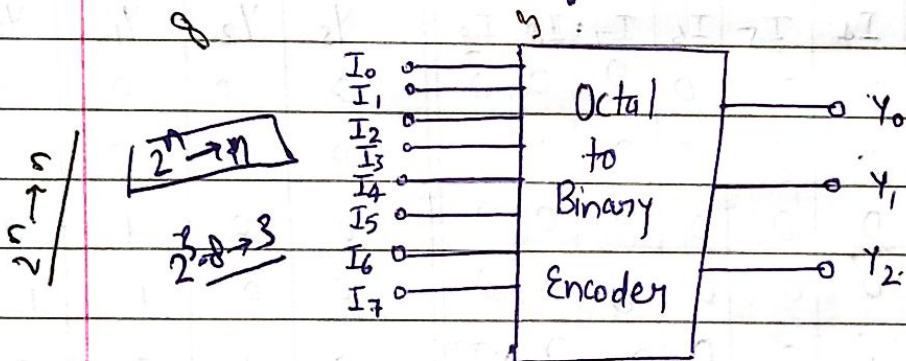
Application of Decoder $\Rightarrow$

- (i) Decoder are used in computer system.
- (ii) They are used in analog to digital converter.
- (iii) Decoder output can be used to drive a display system.

Encoder $\Rightarrow$ An Encoder is a digital circuit that perform the inverse operation of decoder. Hence, the opposite of the decoding process is called encoding.

An Encoder is a combinational logic circuit that convert an active input signal into a coded o/p signal.

- (i) **Octal to Binary Encoder $\Rightarrow$** An octal to binary Encoder perform the 8 bit i/p and



3 bit coded o/p with operation. It accepts 8 I/p and produce a 3 bit o/p code corresponding through the activated i/p.

I/p								o/p		
I ₀	I ₁	I ₂	I ₃	I ₄	I ₅	I ₆	I ₇	Y ₂	Y ₁	Y ₀
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

$$Y_0 = I_1 + I_3 + I_5 + I_7$$

$$Y_1 = I_2 + I_3 + I_6 + I_7$$

$$Y_2 = I_4 + I_5 + I_6 + I_7$$

The truth table of octal to binary encoder and the circuit diagram is shown below.

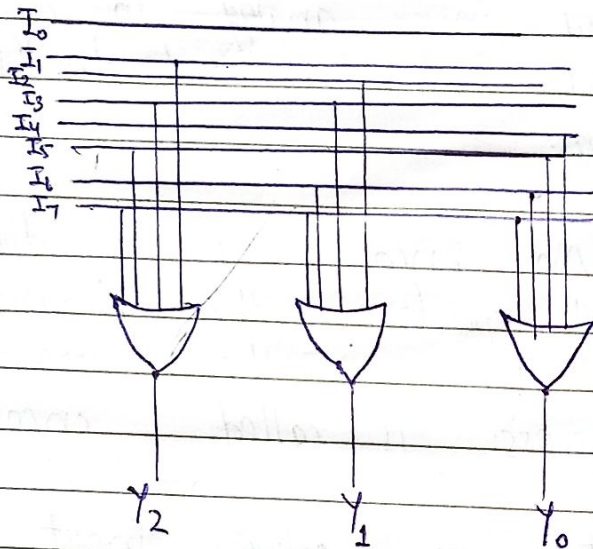


fig:- Octal to binary encoder.

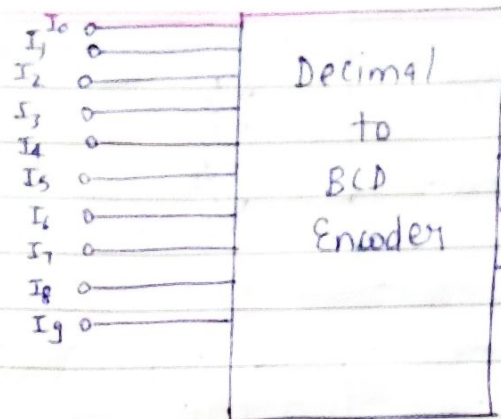
(ii) Decimal to ~~binary~~ BCD Encoder $\Rightarrow$

I/p										o/p			
I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	I_8	I_9	Y_3	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	0	0	1	0	0
0	0	0	0	1	0	0	0	0	0	0	1	1	0
0	0	0	0	0	1	0	0	0	0	0	1	0	1
0	0	0	0	0	0	1	0	0	0	0	1	0	1
0	0	0	0	0	0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	1	0	0	1	1	1
0	0	0	0	0	0	0	0	0	1	0	0	0	0
0	0	0	0	0	0	0	0	0	1	0	0	0	1

(iii)
S.N.

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to binary
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$$\begin{aligned} Y_3 &= I_1 + I_3 + I_5 + I_7 + I_9 \\ Y_2 &= I_2 + I_3 + I_6 + I_7 \\ Y_1 &= I_4 + I_5 + I_6 + I_7 \\ Y_0 &= I_8 + I_9 \end{aligned}$$

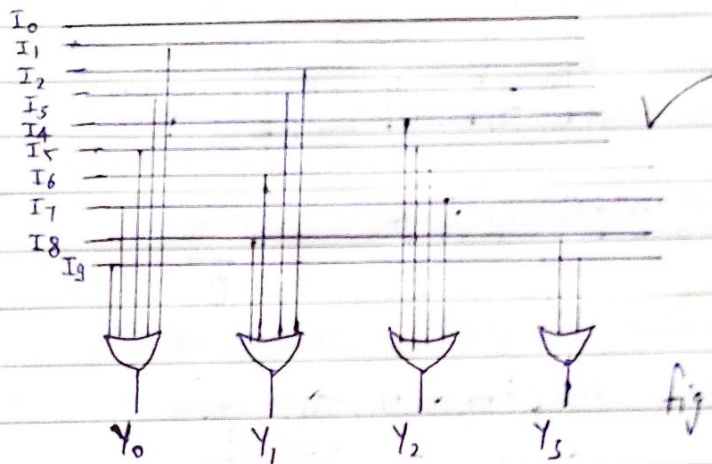
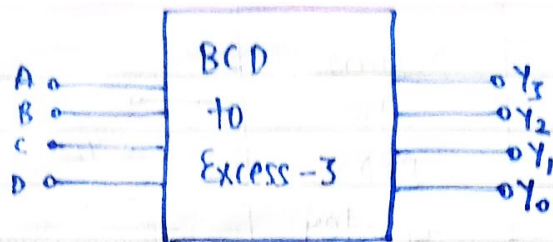


Fig:- Decimal to BCD Encoder

(iii) BCD to Excess-3 encoder $\Rightarrow$

S.N.	BCD				Excess-3			
	A	B	C	D	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1	1
1	0	0	0	1	0	1	0	0
2	0	0	1	0	0	1	0	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	1	1
5	0	1	0	1	1	0	0	0
6	0	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0
8	1	0	0	0	1	0	1	1
9	1	0	0	1	1	1	0	0

Kmap ✓



$Y_0 =$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	5	7	1
11	d	d	d	d
10	1	3	d	d

①

$$Y_0 = \overline{B}\overline{D} + \overline{A}\overline{D}$$

$$Y_0 = \overline{B}\overline{D} = \overline{D}$$

$Y_1 =$

AB \ CD	00	01	11	10
00	1	1	1	1
01	1	5	1	6
11	d	d	d	d
10	1	3	d	d

②

$$Y_1 = \overline{B}\overline{D}\overline{C} + \overline{B}CD = \overline{C}\overline{D} + CD$$

$$Y_1 = \overline{B}(C \oplus D) = C \oplus D$$

$Y_2 =$

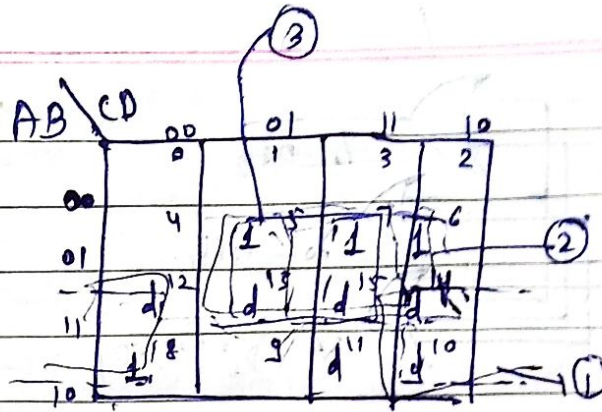
AB \ CD	00	01	11	10
00	1	1	1	1
01	1	5	7	6
11	d	d	d	d
10	1	3	d	d

③

$$Y_2 = \overline{B}\overline{D} + \overline{B}C + B\overline{C}\overline{D} = \overline{B}(C + D) + B(\overline{C} + \overline{D})$$

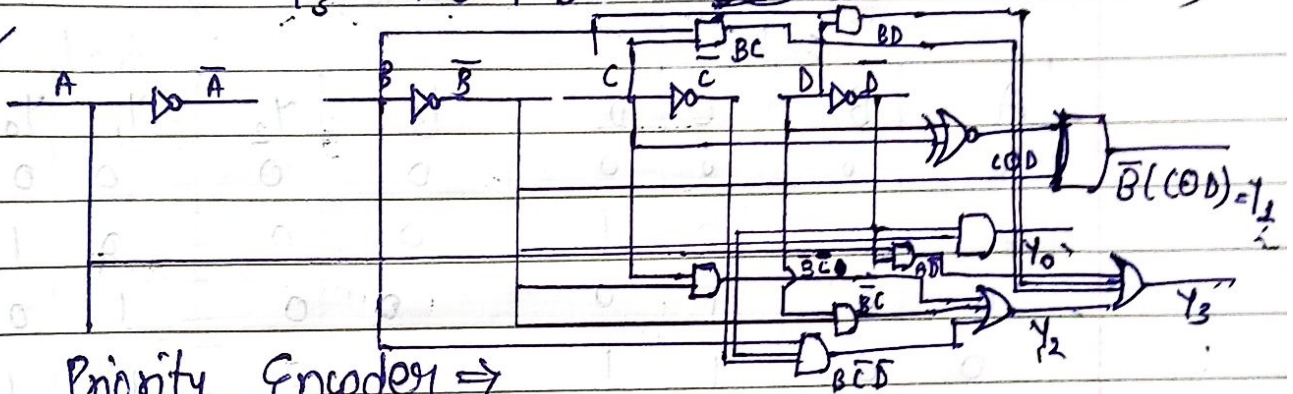
$$= B \oplus (C + D)$$

$Y_3 =$



$$Y_3 = A\bar{D} + BC + \cancel{B\bar{C}D} + BD = A + B(C+D)$$

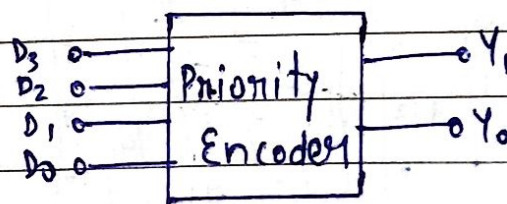
circuit diagram



(iv) Priority Encoder $\Rightarrow$

(a) 4x2 priority Encoder:-

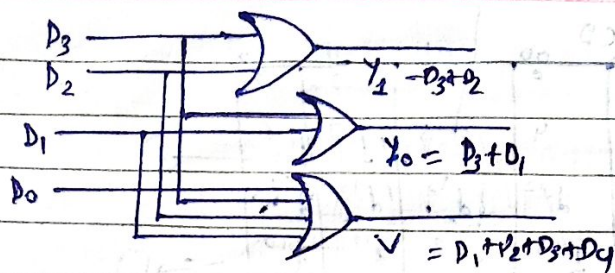
D_3	D_2	D_1	D_0	Y_1	Y_0	V
1	x	x	x	1	1	1
0	1	x	x	1	0	1
0	0	1	x	0	1	1
0	0	0	1	0	0	1
0	0	0	0	d	d	0



$$Y_1 = D_3 + D_2, \quad Y_0 = D_3 + D_1$$

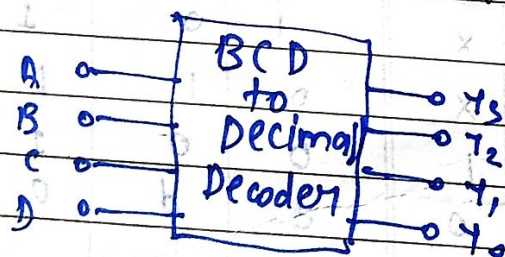
$$V = D_0 + D_1 + D_2 + D_3$$

Date: 4,



BCD to decimal decoder $\Rightarrow$

BCD				Decimal			
A	B	C	D	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	0	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0
0	1	1	1	0	1	1	1
1	0	0	0	1	0	0	0
1	0	0	1	1	0	0	1



$Y_0 =$

AB \ CD	00	01	11	10
00	1	1	1	2
01	1	5	1	6
11	12	13	15	14
10	8	9	11	10

$Y_0 = \overline{B}D$ ✓

$y_1 =$

AB \ CD	00	01	11	10
00	0	1	1	1
01	1	1	1	1
11	d	d	d	d
10	1	1	d	d

$= \overline{A}C$ ✓

$y_2 =$

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	d	d	d	d
10	8	9	d	d

(2)

(1)

$y_2 = BC + BD = B(C+D)$

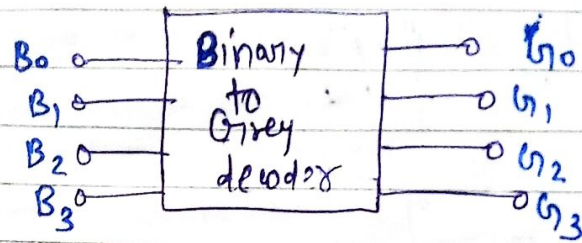
$y_3 =$

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	d	d	d	d
10	8	9	d	d

$\Rightarrow \overline{A}D$

$y_3 y_2 y_1 y_0$ ✓

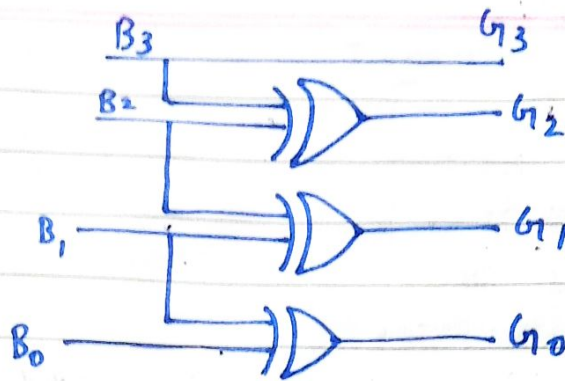
Binary to Gray decoder $\Rightarrow$



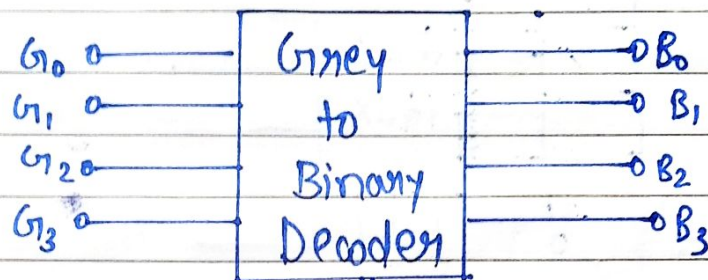
$0 \oplus 1 = 1$
 $1 \oplus 0 = 1$
 $1 \oplus 1 = 0$
 $0 \oplus 0 = 0$

Binary				Gray			
B ₃	B ₂	B ₁	B ₀	G ₃	G ₂	G ₁	G ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

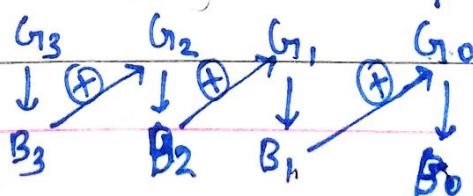
$$\begin{aligned}
 G_3 &\longrightarrow B_3 \\
 G_2 &\longrightarrow B_3 \oplus B_2 \\
 G_1 &\longrightarrow B_2 \oplus B_1 \\
 G_0 &\longrightarrow B_1 \oplus B_0
 \end{aligned}$$



Gray to Binary decoder $\Rightarrow$



Gray				Binary			
G ₃	G ₂	G ₁	G ₀	B ₃	B ₂	B ₁	B ₀
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	0	0
0	1	1	1	0	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	0
1	1	0	1	1	0	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

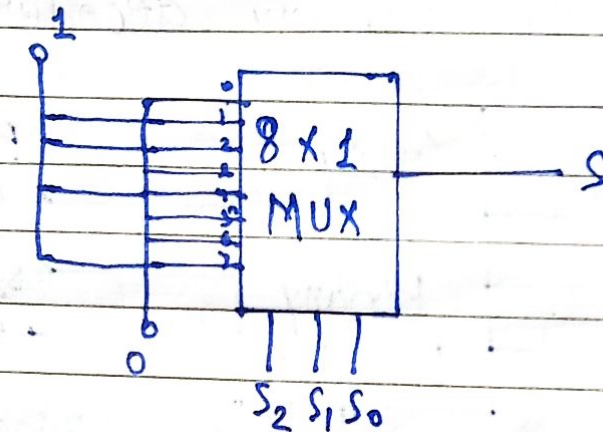


$$\begin{aligned}
 B_3 &\rightarrow G_3 \\
 B_2 &\rightarrow B_3 \oplus G_2 \\
 B_1 &\rightarrow B_2 \oplus G_1 \\
 B_0 &\rightarrow B_1 \oplus G_0
 \end{aligned}$$

Implement

Q. $S = \sum m(1, 2, 4, 7)$ solve using 8×1 MUX

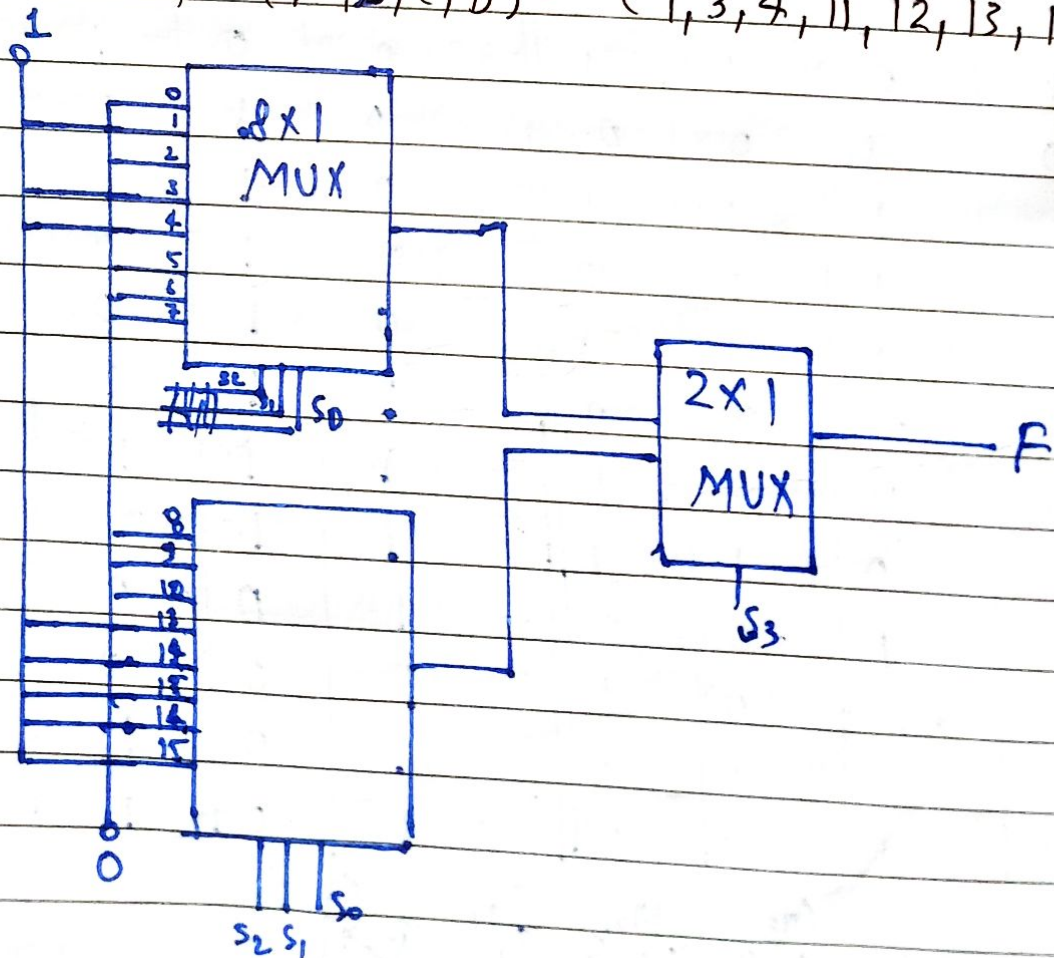
Ans -



Q. Implement the following function using 8×1 MUX.

$$F(A, B, C, D) = \sum m(1, 3, 4, 11, 12, 13, 14, 15)$$

Ans -



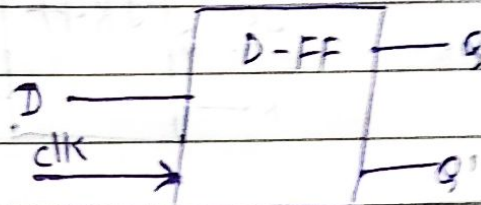
Unit - 5

Flip-Flop

Flip-flop is used to store the memory of 1 bit.

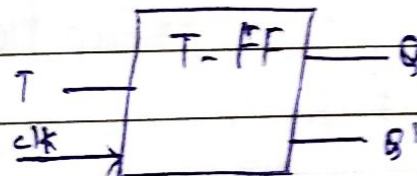
Type of Flip-flop : —

(i) D - flip flop : —



clk	I/P (D)	O/P (Q)
0	0	0
1	1	1

(ii) T - flipflop : —



clk	I/P (T)	O/P (Q)
0	0	1
1	1	0



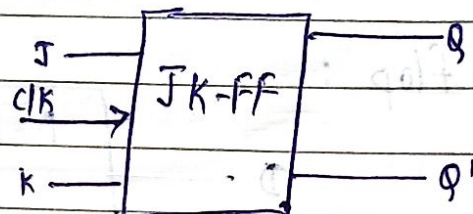
T-FF using D-FF

(iii) SR - flipflop : —



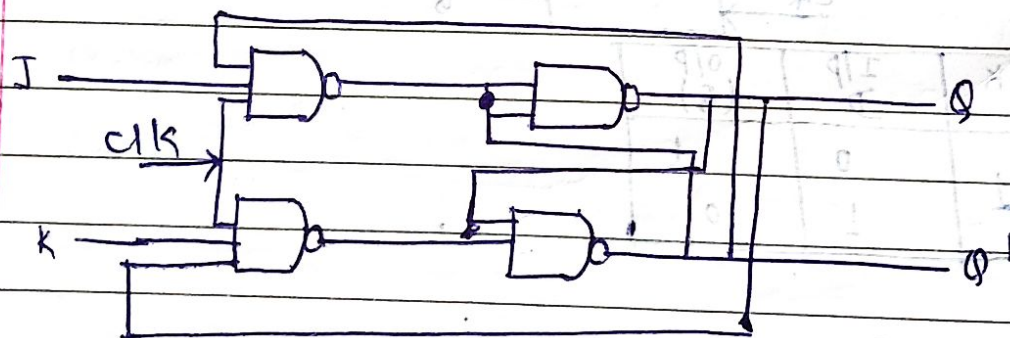
clk	I/p		O/p	Comment
	S	R	Q	
1	0	0	Q	Previous
	0	1	0	Reset
	1	0	1	Set
	1	1	?	Not Define

(iv) **JK - flip flop :-**



clk	I/p		O/p	Comment
	J	k	Q	
1	0	0	Q	Previous
	0	1	0	Reset
	1	0	1	set
	1	1	Q	Toggle

The limitation of SR flip flop is overcome in JK flip flop.

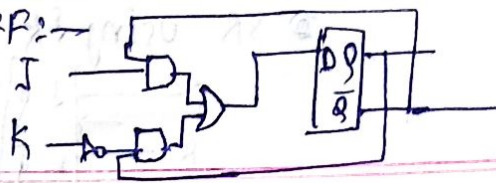


(i) At 0, 0 input o/p will be Q and comment will be previous.

(ii) If J i/p is 0 & K i/p is 1 then o/p will be 0 & comment will be reset.

(iii) If J i/p is 1 & K i/p is 0 then o/p will be 1 & comment will be set.

JK using D-FF:-



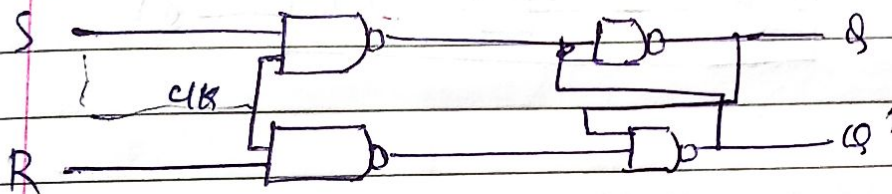
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Page No. : 11/
Date :

(iv) If J & K is 1 input then o/p will be $\bar{Q}$ and comment will be Toggle.

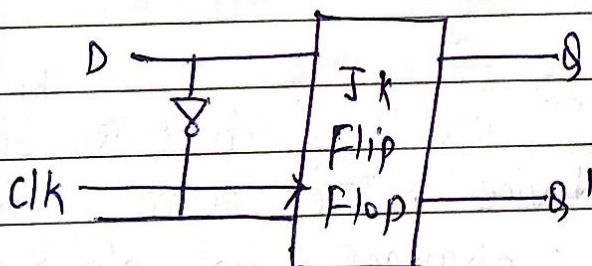
SR-flip flop:-

SR Flip flop will be set or reset anytime by changing the inputs S & R. Most of the application demand the memory cell to set or reset in synchronous with the clock.



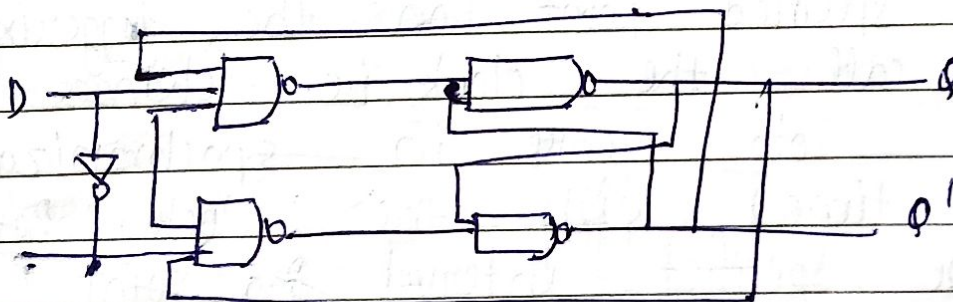
or SR

① D-flip flop using JK flip flop:-



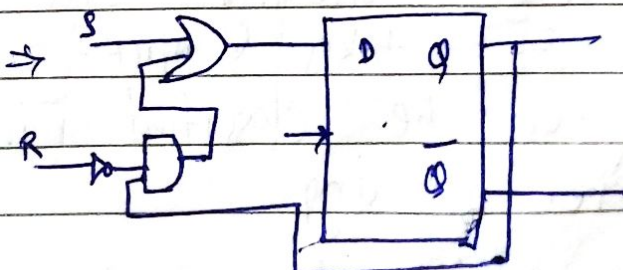
I/p	O/p
0 0	0
0 1	0
1 0	1
1 1	0

I/P	O/P
0	0
1	1

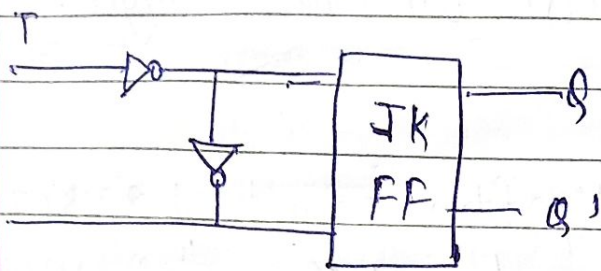


using
DFF & SRFF

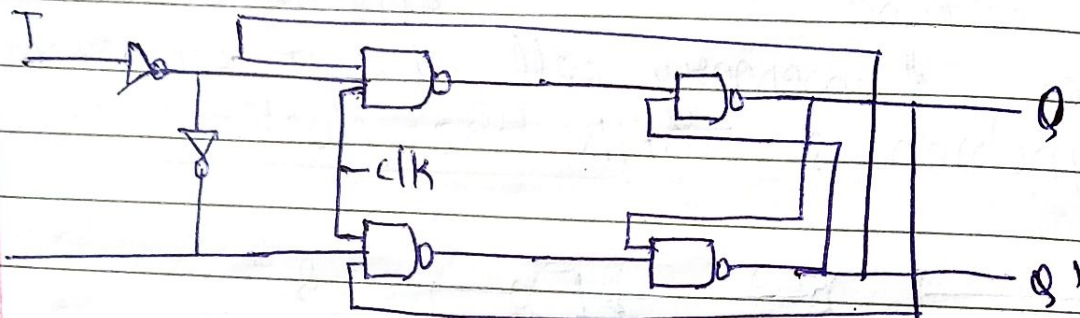
SR using D-FF



② T-FF using JK-FF:—



I/p	O/p
0	1
1	0



Triggering of Flip flop:—

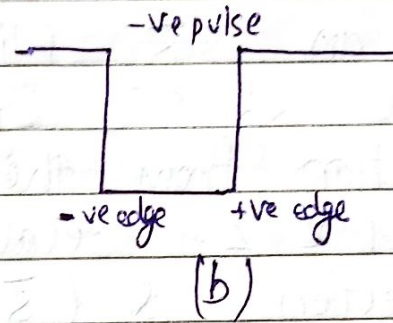
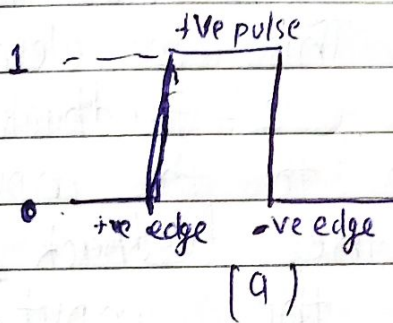
- Level Triggering
- Edge Triggering

① ~~Level~~ Triggering $\Rightarrow$ FF are ^{by stable} synchronous bias level device. The term synchronous means that the changes in o/p across the specified point on the triggering i/p call the clock i.e. changes in the o/p across in synchronization (in time) with the clock. Based on the specified interval or point in the clock during ^{at} which triggering of FF takes place. It can be classified into 2 type:—

- (i) level triggering
- (ii) Edge triggering

(i) Level Triggering $\Rightarrow$ When the clk pulse goes high then the FF is said to be level trigger FF. Since the FF change its state when the clk is positive it is termed as positive level trigger FF. The FF changes its state only when the clk is negative it is called -ve level trigger FF.

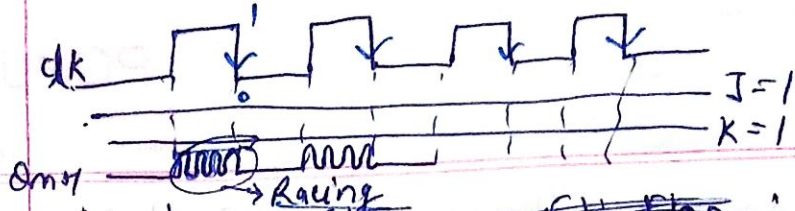
(ii) Edge Triggering $\Rightarrow$



The term Edge triggering means that the FF changes its state either at the +ve edge (rising or leading edge) or at the -ve edge (falling or trailing edge) of the clk pulse and is sensitive to its input on at this transmission of the clk.

Application of Flip Flop

- (i) Tabular data storage
- (ii) shift register
- (iii) frequency division
- (iv) Counter



~~Master-Slave Flip Flop :-~~

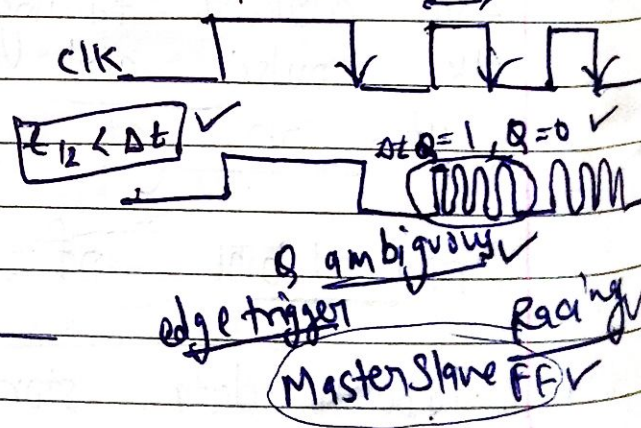
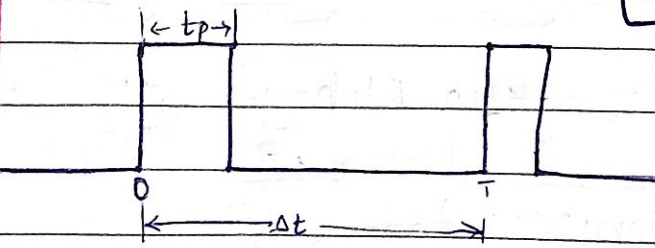
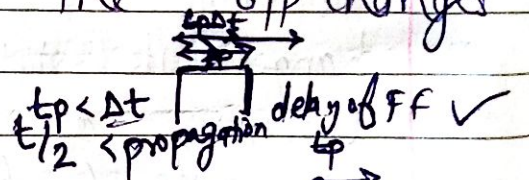
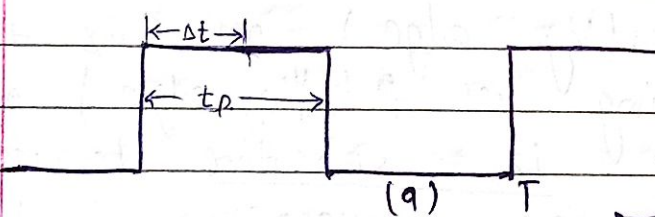
~~The Race around condition~~

Before the development of edge trigger FF The timing problem in level trigger FF was ~~not~~ often handled by Master slave FF.

Race Around condition :-

The condition $S=1$ and $R=1$, we have seen is not allowed in an SR Flip Flop. This is eliminated in the JK FF by using the feedback connection from the output to the inputs of gate 1 & 2. Because of the feedback connection Q ($\bar{Q}$) at the input K (J), the input will be changed during the clock pulse ($clk=1$), if the o/p changes the state.

~~toggle~~



For example, that the inputs are $J=K=1$ and $Q=0$. When a clk pulse with t_p as shown in figure (a) is applied the i/p will

- (i) $T/2 < \text{propagation delay of FF}$
- (ii) edge trigger
- (iii) master slave FF

change from 0 to 1 after a time interval Δt where Δt is the propagation delay through two NAND gate series.

After ~~some~~ time Δt , we have $J=K=1$ and $Q=1$ and after another interval of Δt o/p Q will become 0. Hence the o/p will oscillate back and forth b/w 0 & 1. In the duration t_p of the clk pulse width. So at the end of the clk pulse the value Q is ambiguous. This situation is known as the race around condition.

The race around condition can be avoided if $t_p < \Delta t$ as shown in figure (b). Lumped delay line can be used in series with the delay condition in order to increase the loop delay beyond t_p and hence to prevent the race around condition. The race around condition can be avoided in master slave FF.

Master slave Flip-flop $\Rightarrow$ This FF design using 2 separate FF connected serially. The first FF serve as the master and the second Flip-flop as the slave. And they overall circuit refer to as master slave FF.

Master slave FF is same as -ve edge trigger.

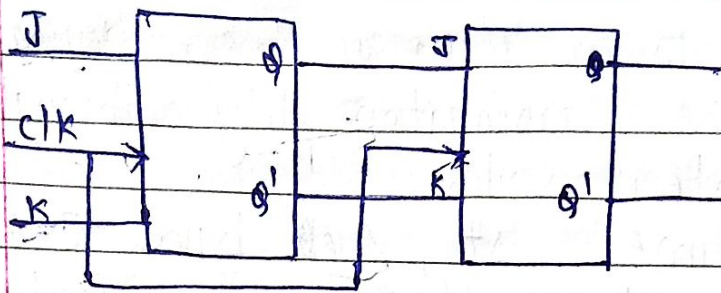
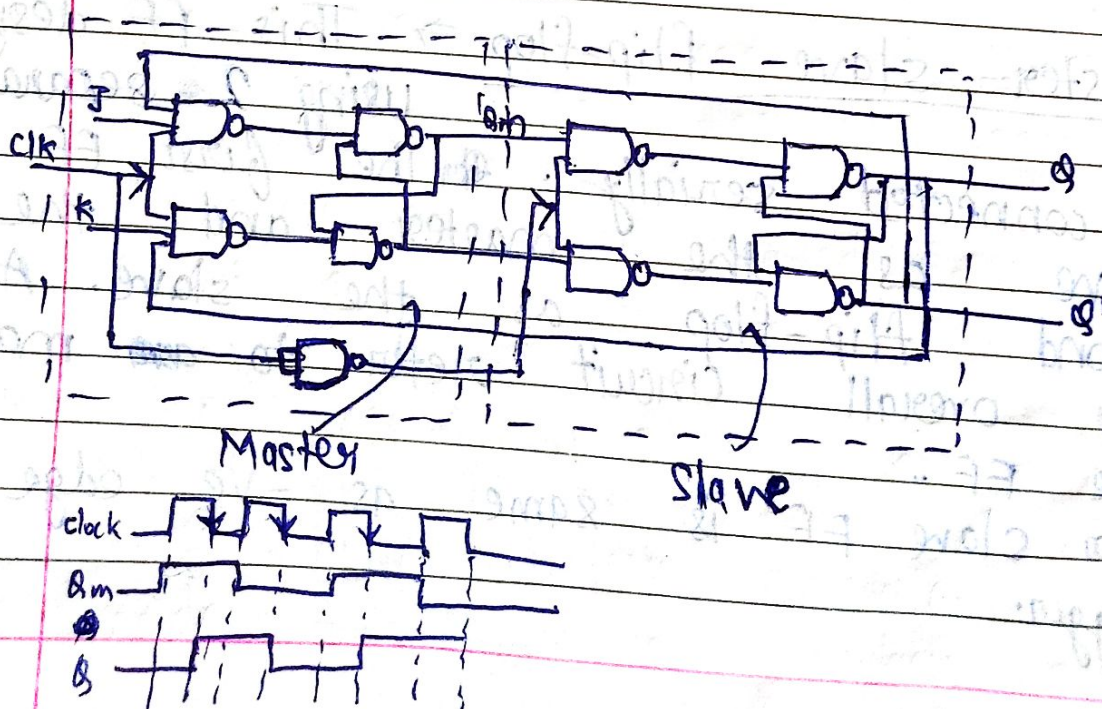


Fig:- Master slave flip flop

The first FF can be hold the master is driven by positive edge of the clock pulse. The second FF hold the slave is driven by negative edge of the clock pulse. Therefore when the clk input as a positive edge, the master^{get} according to its JK input. When the clk input has a negative edge the slave FF copy the master FF outputs. But the master does not copy or respond to the feedback from Q & Q'. Since it requires positive edge at its clk i/p. ~~do~~ Thus ~~does~~ master slave FF doesn't has race around problem.



Operation of Master Slave FF $\Rightarrow$

- (i) If $J=1$ & $K=0$ the master FF set on the +ve edge clk. The high Q_1 o/p of the master driven the i/p of the slave. So when the -ve clk edge hits the slave also set. The slave FF copies the action of master FF.
 - (ii) If $J=0$ & $K=1$ the master reset on the leading edge of clk pulse. The o/p Q_1 is high of the master drive of the i/p K of slave FF. Then the slave FF reset at the arrival of the falling/trailing edge of clk pulse. Once again the slave FF copy the action of master FF.
 - (iii) If $J=K=1$ the master FF toggles on the +ve edge clk and the slave toggles on the -ve edge clk. The condition $J=K=0$ input does not produce any changes.
- Master slave FF operate from a complete clk pulse and the o/p change on the negative transmission.

COUNTER $\Rightarrow$ A counter by function is a sequential circuit consist a set of FF connecting in a suitable manner to count the sequence of the input pulse presented to it in digital form.

Counter can be classified into 3 category:—

- (i) Synchronous & Asynchronous counter
- (ii) Single & Multiple counter
- (iii) Modulus counter

(i) Asynchronous counter:—

An asynchronous counter or ripple counter can be designed using minimum h/w. In an asynchronous counter each flip flop is ~~each~~ toggled by the output from the previous FF which limit its speed of operation. The settling time in asynchronous counter is the commulating sum of the individual settling time of the FF. It is also called serial counter.

Synchronous counter:—

In synchronous counter the speed limitation of ripple counter is overcome by applying clock pulse to all together Flip flop which leads the settling time of the counter being equal to the propagation delay of a single ff. Hence, synchronous counter is also called parallel counter.

(ii) Single mode counter & multimode counter

Single mode counters operate in a single mode. It counts either in the up

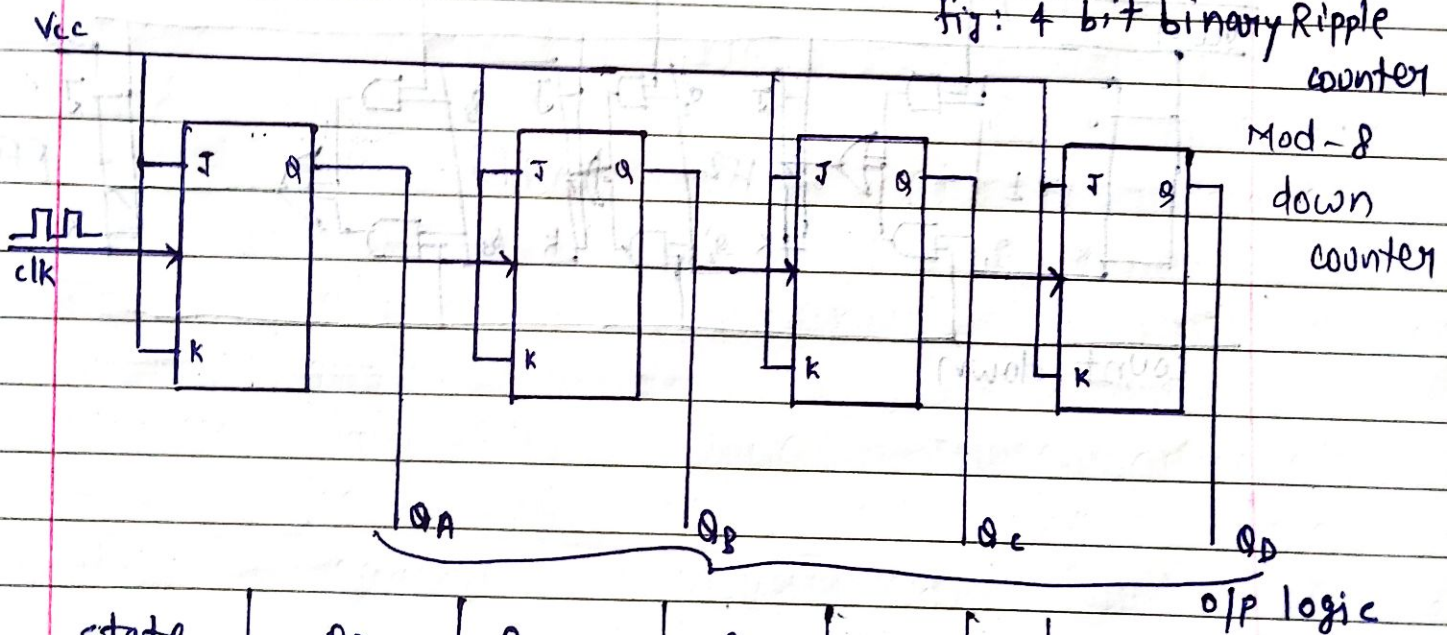
mode or in down mode. Whenever multi mode counters operate in both (up mode & down mode).

(iii) Modulus Counter : —
(Mode counter)

Modulus counter are defined based on the no. of states, they are capable of counting. For example a ~~MODE~~ MODE 10 counter has 10 states.

Asynchronous (ripple or serial) counter : —

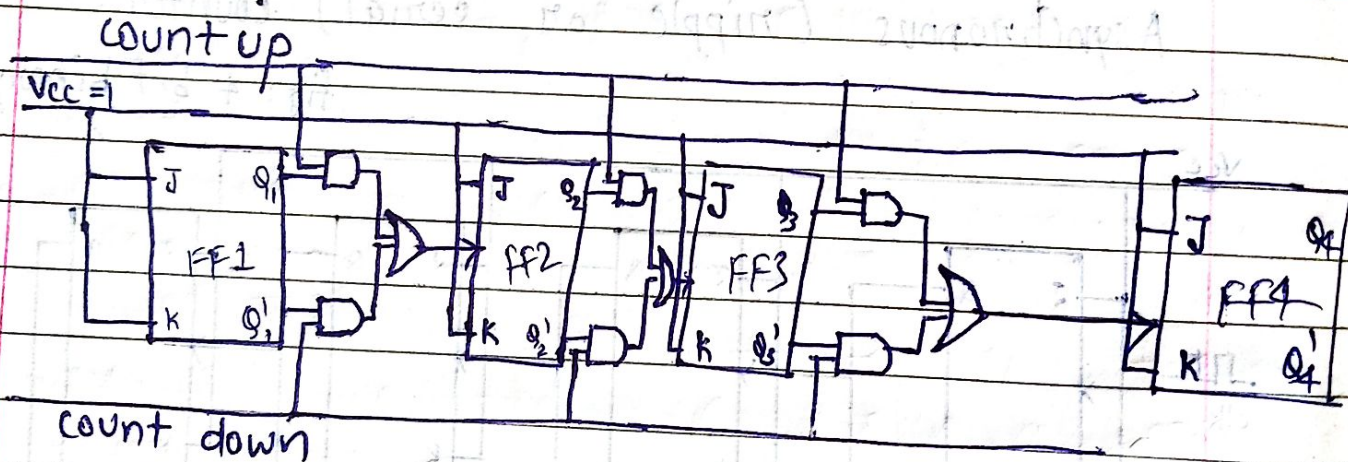
fig: 4 bit binary Ripple counter



state	Q_D	Q_C	Q_B	Q_A	state
0	0	0	0	0	15
1	0	0	0	1	14
2	0	0	1	0	13
3	0	0	1	1	12
4	0	1	0	0	11
5	0	1	0	1	10
6	0	1	1	0	9

7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	0	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
0	0	0	0	0

UP - DOWN COUNTER $\Rightarrow$



Design of synchronous counter $\Rightarrow$

This step involves in design of synchronous counter are given below:—

Step-1 Draw state diagram which describe the operation of counter

Step-2 From the above state diagram obtain present state (PS) & next state (NS) ~~table~~ table of the counter and check the whenever it has any equivalent state. Any two states are said to be equivalent if and only if their next state are 1 and the same. In such a case one of the equivalent state can be eliminated from state table. Thus in this state step the state is modified in such a way that there is no detectant state redundant state in it.

Step-3 Make a state assignment & document the same in above state table.

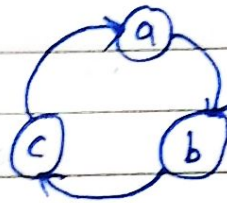
Step-4 Beside the type of memory element to be used and then obtain the excitation table from PS, NS table using the application table of the FF.

Step-5 Draw the excitation map for various excitation input of the FF and simplify the excitation function.

Step-6 Draw the systematic diagram of the counter.

MOD-3 Counter $\Rightarrow$

(i) $a \rightarrow b \rightarrow c \rightarrow a$
state diagram:—

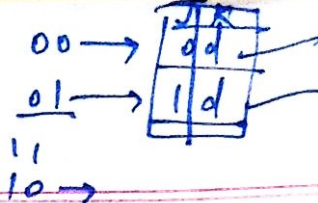


(ii) State table (PS-NS) of MOD-3 counter:—

P.S.	N.S.
a	b
b	c
c	a

(iii) State assignment:—

P.S.		N.S.	
z_1	z_0	q_1	q_0
0	0	0	1
0	1	1	0
1	0	0	0
1	1	d	d

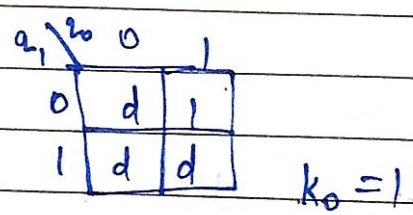
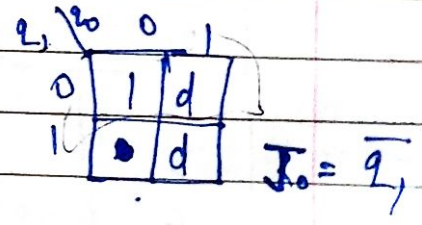
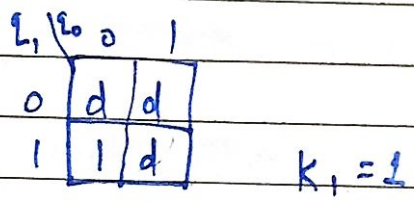
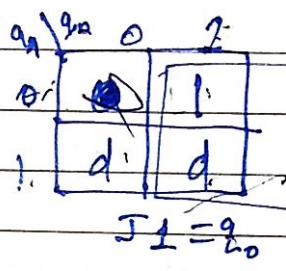


(iv) Excitation table:—

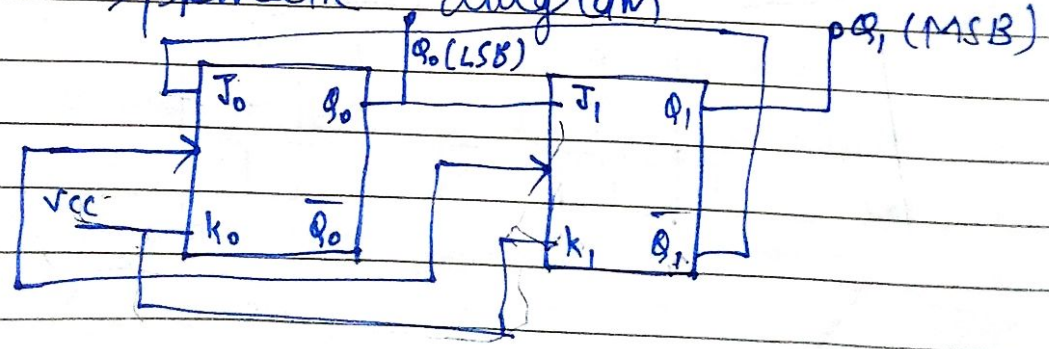
P.S.		N.S.		Excitation Inputs			
Q_1	Q_0	Q_1	Q_0	J_1	K_1	J_0	K_0
0	0	0	1	0	d	1	d
0	1	1	0	1	d	d	1
1	0	0	0	d	1	0	d
1	1	d	d	d	d	d	d

00 → 0d
01 → 1d
10 → d1
11 → dd

(v) Excitation Map:—



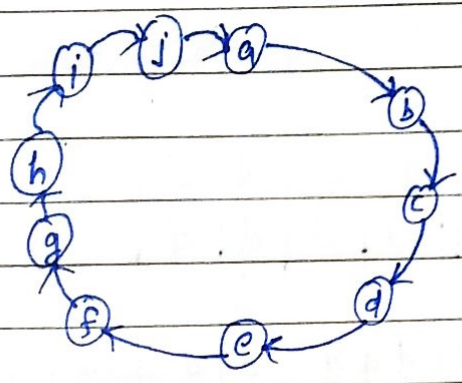
(vi) Systematic diagram



MOD - 10 Counter :-

(i) State - Diagram $\Rightarrow$

a, b, c, d, e, f, g, h, i, j
state



(ii) State table (PS-NS) of MOD - 10 counter $\Rightarrow$

P.S.	N.S.
a	b
b	c
c	d
d	e
e	f
f	g
g	h
h	i
i	j
j	a

(iii) State assignment of MOD - 10 counter $\Rightarrow$

P.S.				N.S			
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0

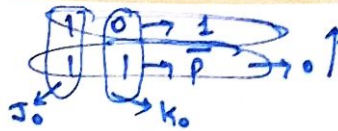
0	0	0	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0
1	0	1	0	d	d	d	d
1	0	1	1	d	d	d	d
1	1	0	0	d	d	d	d
1	1	0	1	d	d	d	d
1	1	1	0	d	d	d	d
1	1	1	1	d	d	d	d

$$\left[\begin{array}{cc|cc} & & & \\ 0 & 0 & \rightarrow & 0 & d \\ 0 & 1 & \rightarrow & 1 & d \\ 1 & 0 & \rightarrow & d & 1 \\ 1 & 1 & \rightarrow & d & a \end{array} \right] \quad \begin{array}{l} T \\ K \\ \\ V \end{array}$$

(iv) Excitation Table $\Rightarrow$

[illegible]

0,1



0/0	→ Previous
0/0	→ 0
1/0	→ 1
1/1	→ Toggle

1	1	0	0	d	d	d	d	d	d	d	d	d	d	d	d
1	1	0	1	d	d	d	d	d	d	d	d	d	d	d	d
1	1	1	0	d	d	d	d	d	d	d	d	d	d	d	d
1	1	1	1	d	d	d	d	d	d	d	d	d	d	d	d

(v) Excitation Map:—

for $J_3 =$

$q_3 q_2$	$q_1 q_0$	00	01	11	10
00	0	1	3	2	
01	4	5	7	6	
11	d ¹²	d ¹³	d ¹⁵	d ¹⁴	
10	d ⁸	d ⁹	d ¹¹	d ¹⁰	

$$J_3 = q_2 q_1 q_0 \checkmark$$

for $K_3 =$

$q_3 q_2$	$q_1 q_0$	00	01	11	10
00	d ⁰	d ¹	d ³	d ²	
01	d ⁴	d ⁵	d ⁷	d ⁶	
11	d ¹²	d ¹³	d ¹⁵	d ¹⁴	
10	d ⁸	d ⁹	d ¹¹	d ¹⁰	

$$K_3 = \underline{q_0}$$

for $J_2 =$

$q_3 q_2$	$q_1 q_0$	00	01	11	10
00	0	1	3	2	
01	d ⁴	d ⁵	d ⁷	d ⁶	
11	d ¹²	d ¹³	d ¹⁵	d ¹⁴	
10	d ⁸	d ⁹	d ¹¹	d ¹⁰	

$$\underline{q_1 q_0}$$

and so on:—

$$K_2 = q_1 q_0$$

$$J_1 = \underline{q_3 q_0}$$

$$K_1 = \underline{q_0}$$

$$J_0 = 1$$

$$K_0 = 1$$

for $k_2 =$

	$q_3 q_2$	$q_1 q_0$	01	11	10
q_3	0	1	d	3	2
q_2	d	d	5	7	6
01	d	12	d	13	d
11	d	8	d	9	d
10	d	d	d	d	d

$$q_1 q_0 \bar{q}_2 = q_1 q_0$$

(v)

 $V_{CC} = 1$

for $J_1 =$

	$q_3 q_2$	$q_1 q_0$	01	11	10
q_3	0	1	1	d	d
q_2	d	4	1	5	d
01	d	12	d	13	d
11	d	8	d	9	d
10	d	d	d	d	d

$$\bar{q}_3 q_0$$

for $k_1 =$

	$q_3 q_2$	$q_1 q_0$	01	11	10
q_3	0	1	d	3	2
q_2	d	d	5	7	6
01	d	12	d	13	d
11	d	8	d	9	d
10	d	d	d	d	d

$$\bar{q}_2 q_0 = q_0$$

for $J_0 =$

	$q_3 q_2$	$q_1 q_0$	01	11	10
q_3	0	1	d	3	2
q_2	d	4	d	5	d
01	d	12	d	13	d
11	d	8	d	9	d
10	d	d	d	d	d

$$= 1$$

for $k_0 =$

	$q_3 q_2$	$q_1 q_0$	01	11	10
q_3	0	1	1	3	d
q_2	d	4	1	5	d
01	d	12	d	13	d
11	d	8	d	9	d
10	d	d	d	d	d

$$= L$$

$K_0 = 1, J_0 = 1, K_1 = Q_0, J_1 = \bar{Q}_0, K_2 = Q_1, J_2 = \bar{Q}_1, K_3 = Q_2, J_3 = \bar{Q}_2$

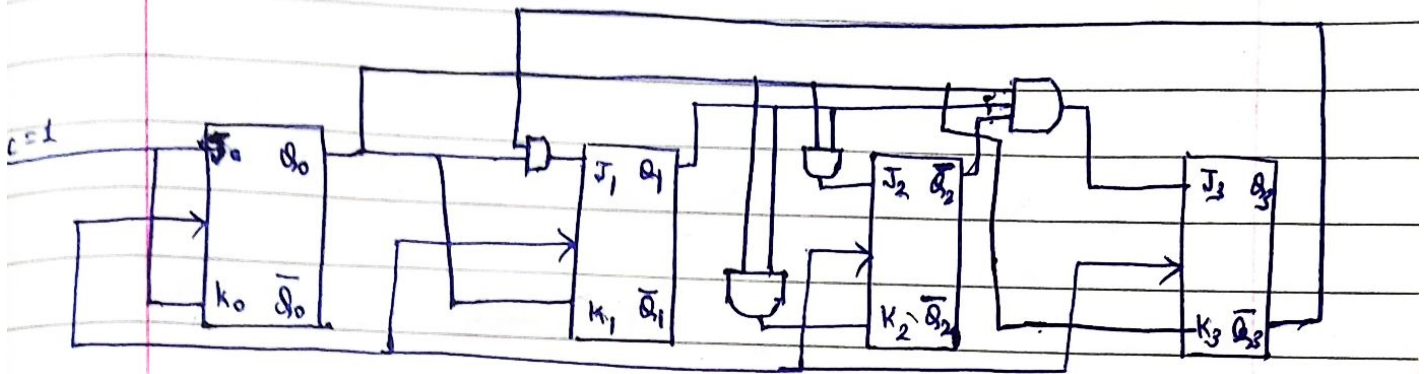
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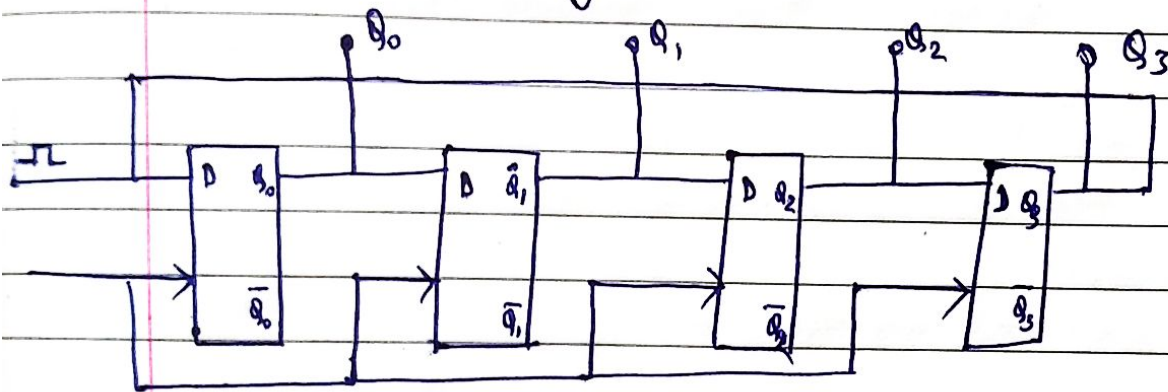
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(vi) System diagram:—

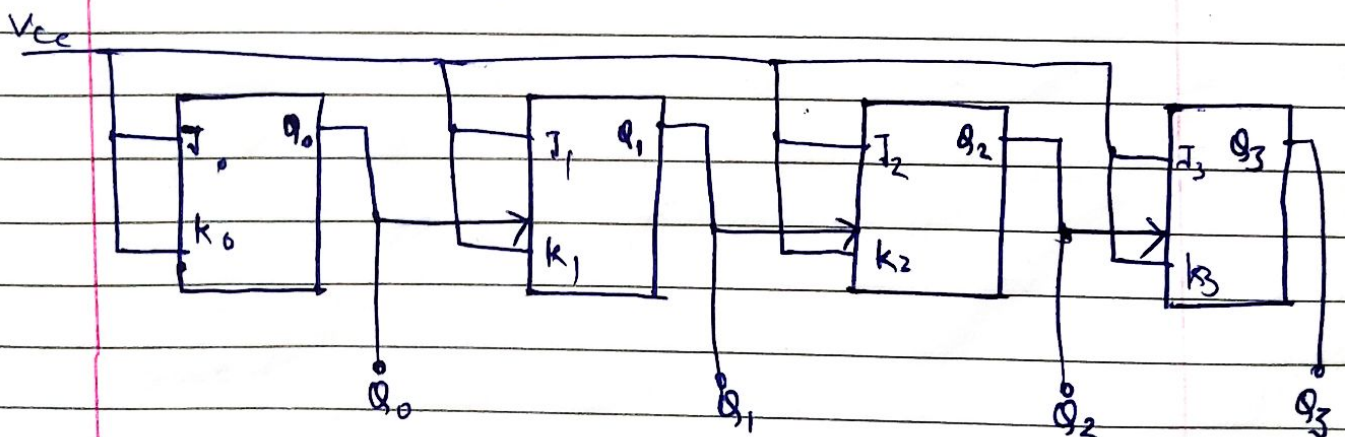
$K_3 = Q_0, J_3 = \bar{Q}_0, K_4 = Q_1, J_4 = \bar{Q}_1, K_5 = Q_2, J_5 = \bar{Q}_2$



4 - Bit Ring counter $\Rightarrow$



4 - Bit Binary counter $\Rightarrow$



Shift Register

A group of flip flops which is used to store multiple bits of data and the data is moved from one flip flop to another is known as **Shift Register**. The bits stored in registers shifted when the clock pulse is applied within and inside or outside the registers. To form an n-bit shift register, we have to connect n number of flip flops. So, the number of bits of the binary number is directly proportional to the number of flip flops. The flip flops are connected in such a way that the first flip flop's output becomes the input of the other flip flop.

A **Shift Register** can shift the bits either to the left or to the right. A **Shift Register**, which shifts the bit to the left, is known as "**Shift left register**", and it shifts the bit to the right, known as "**Right left register**".

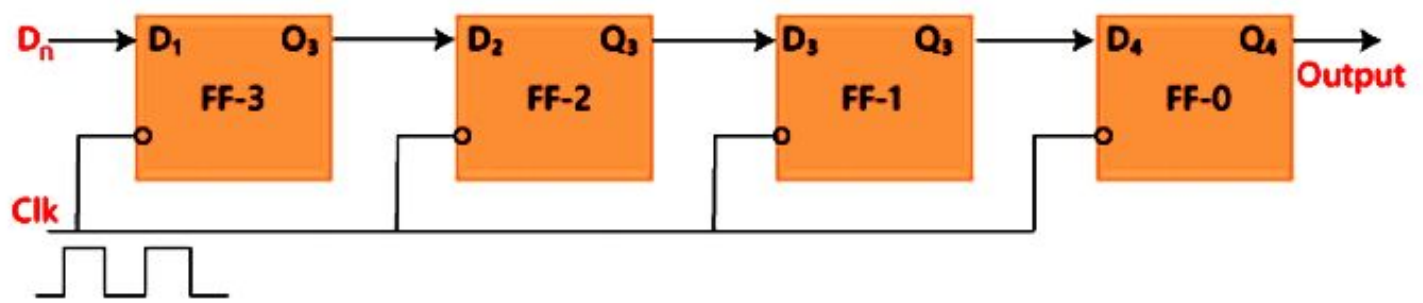
The shift register is classified into the following types:

- Serial In Serial Out
- Serial In Parallel Out
- Parallel In Serial Out
- Parallel In Parallel Out
- Bi-directional Shift Register
- Universal Shift Register

Serial IN Serial OUT

In "Serial Input Serial Output", the data is shifted "IN" or "OUT" serially. In SISO, a single bit is shifted at a time in either right or left direction under clock control.

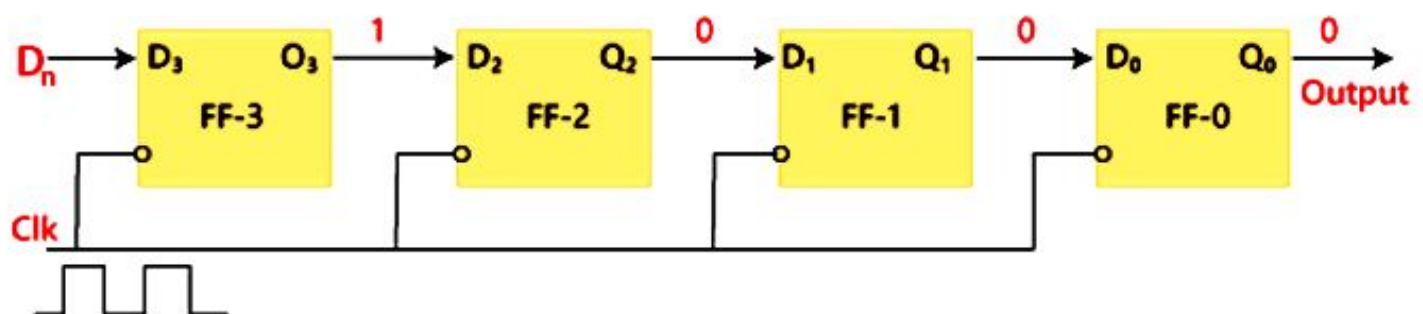
Initially, all the flip-flops are set in "reset" condition i.e. $Y_3 = Y_2 = Y_1 = Y_0 = 0$. If we pass the binary number 1111, the LSB bit of the number is applied first to the Din bit. The D3 input of the third flip flop, i.e., FF-3, is directly connected to the serial data input D3. The output Y_3 is passed to the data input d_2 of the next flip flop. This process remains the same for the remaining flip flops. The block diagram of the "**Serial IN Serial OUT**" is given below.



Operation

When the clock signal application is disabled, the outputs $Y_3 Y_2 Y_1 Y_0 = 0000$. The LSB bit of the number is passed to the data input D_{in} , i.e., D_3 .

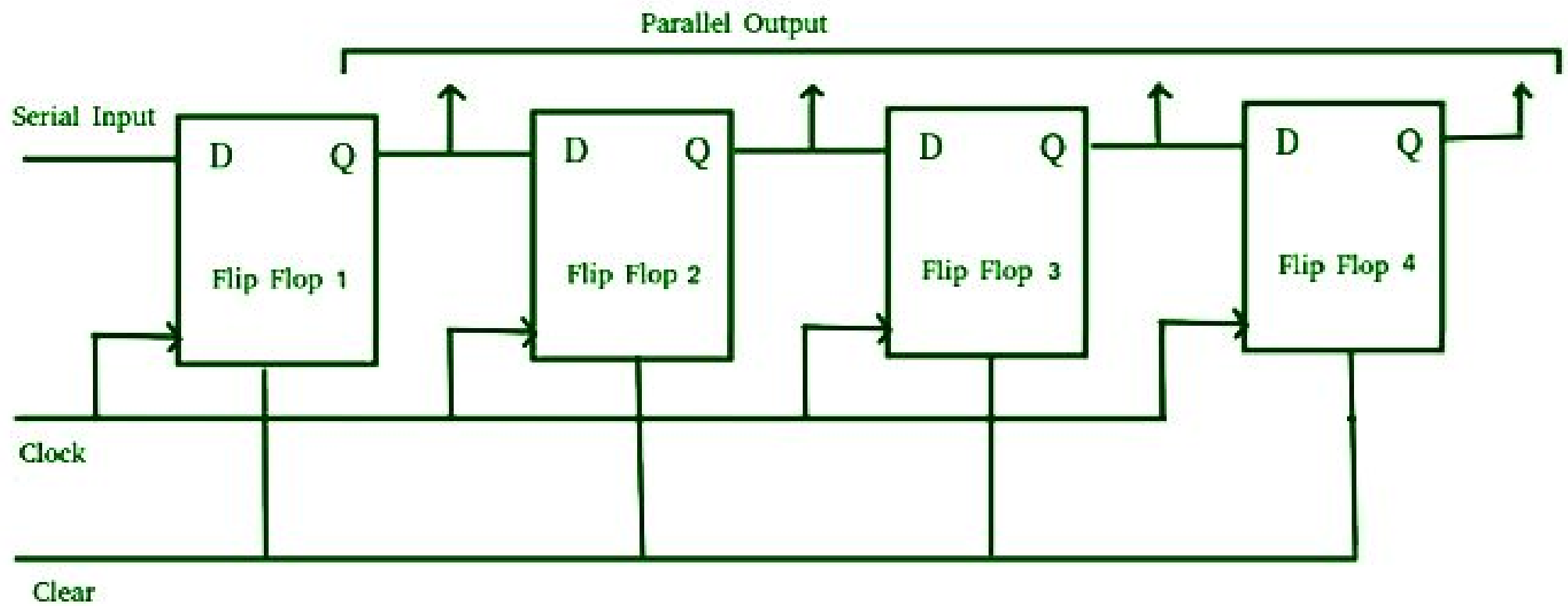
We will apply the clock, and this time the value of D_3 is 1. The first flip flop, i.e., FF-3, is set, and the word is stored in the register at the first falling edge of the clock. Now, the stored word is 1000.



Serial-In Parallel-Out shift Register (SIPO) –

The shift register, which allows serial input (one bit after the other through a single data line) and produces a parallel output is known as Serial-In Parallel-Out shift register.

The logic circuit given below shows a serial-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal is connected in addition to the clock signal to all the 4 flip flops in order to RESET them. The output of the first flip flop is connected to the input of the next flip flop and so on. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip flop.

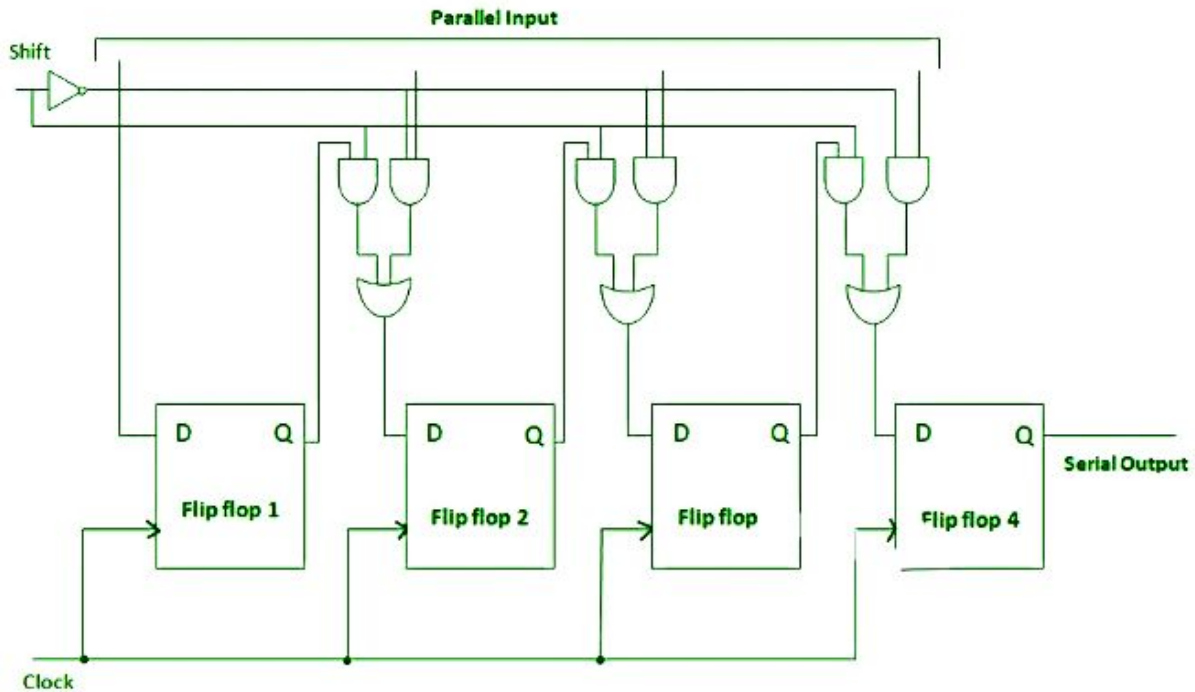


Parallel-In Serial-Out Shift Register (PISO) –

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and produces a serial output is known as Parallel-In Serial-Out shift register.

The logic circuit given below shows a parallel-in-serial-out shift register. The circuit consists of four D flip-flops which are connected. The clock input is directly connected to all the flip flops but the input data is connected individually to each flip flop through a multiplexer at the input of every flip flop. The output of the previous flip flop and parallel data input are connected to the input of the MUX and the output of MUX is connected to the next flip flop. All these flip-flops are synchronous with each other since the same clock signal is applied to each flip

flop.

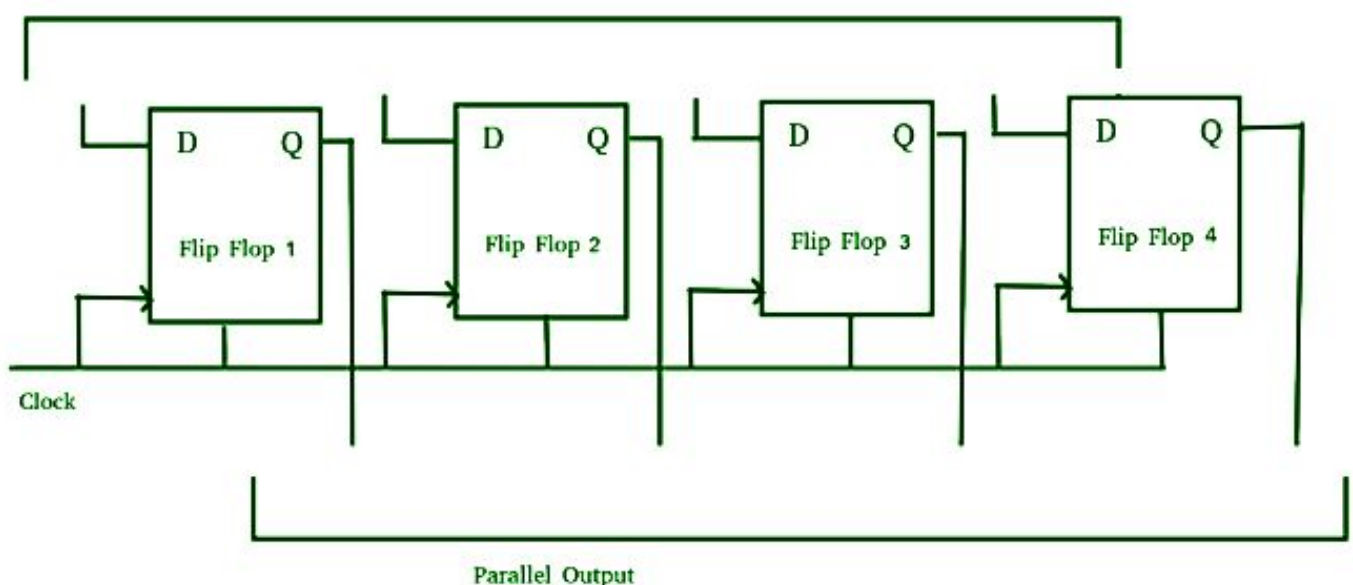


A Parallel in Serial out (PISO) shift register is used to convert parallel data to serial data.

Parallel-In Parallel-Out Shift Register (PIPO) –

The shift register, which allows parallel input (data is given separately to each flip flop and in a simultaneous manner) and also produces a parallel output is known as Parallel-In parallel-Out shift register.

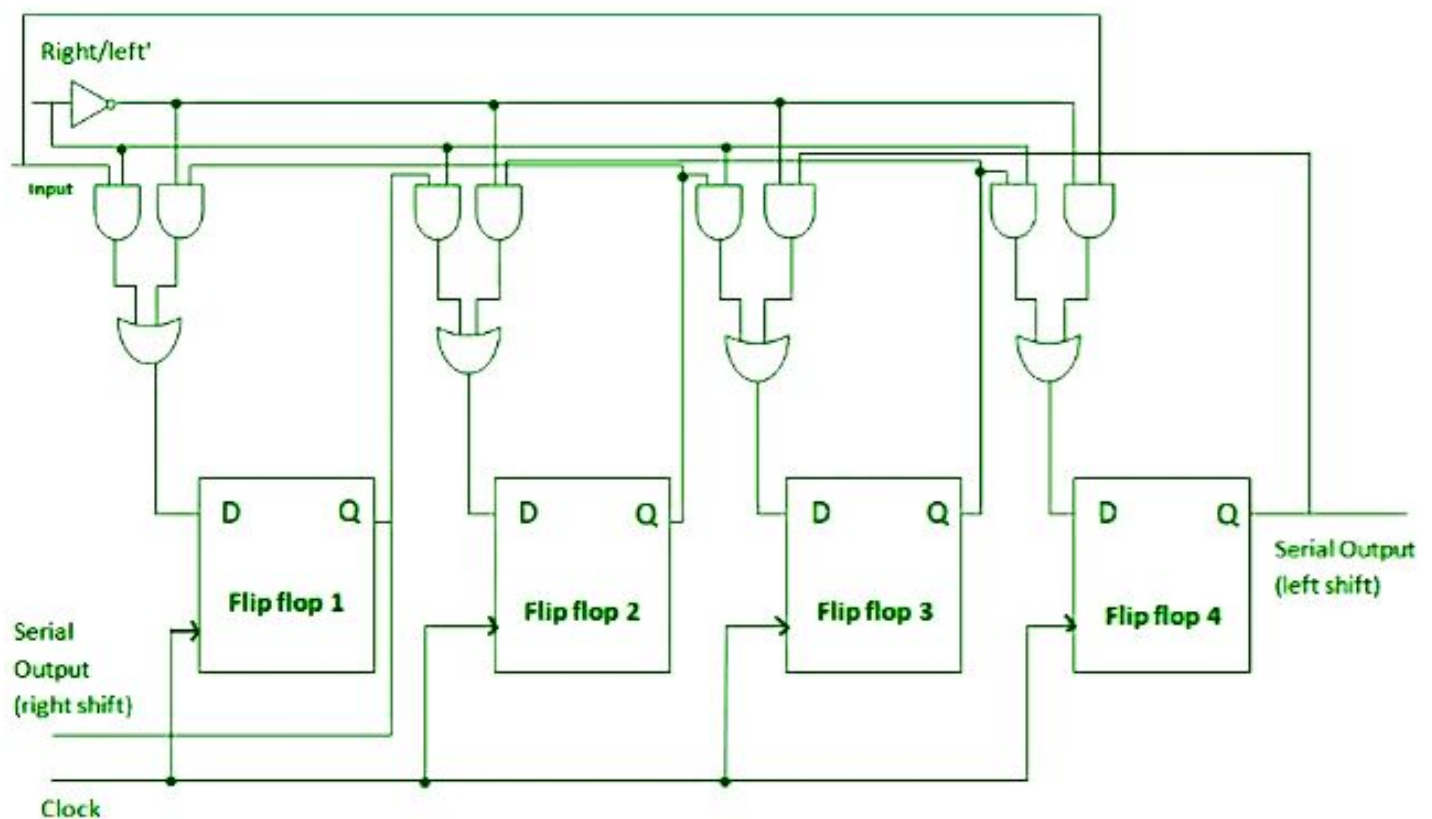
The logic circuit given below shows a parallel-in-parallel-out shift register. The circuit consists of four D flip-flops which are connected. The clear (CLR) signal and clock signals are connected to all the 4 flip flops. In this type of register, there are no interconnections between the individual flip-flops since no serial shifting of the data is required. Data is given as input separately for each flip flop and in the same way, output also collected individually from each flip flop.



Bidirectional Shift Register –

If we shift a binary number to the left by one position, it is equivalent to multiplying the number by 2 and if we shift a binary number to the right by one position, it is equivalent to dividing the number by 2. To perform these operations we need a register which can shift the data in either direction.

Bidirectional shift registers are the registers which are capable of shifting the data either right or left depending on the mode selected. If the mode selected is 1 (high), the data will be shifted towards the right direction and if the mode selected is 0 (low), the data will be shifted towards the left direction.



Shift Register Counter –

Shift Register Counters are the shift registers in which the outputs are connected back to the inputs in order to

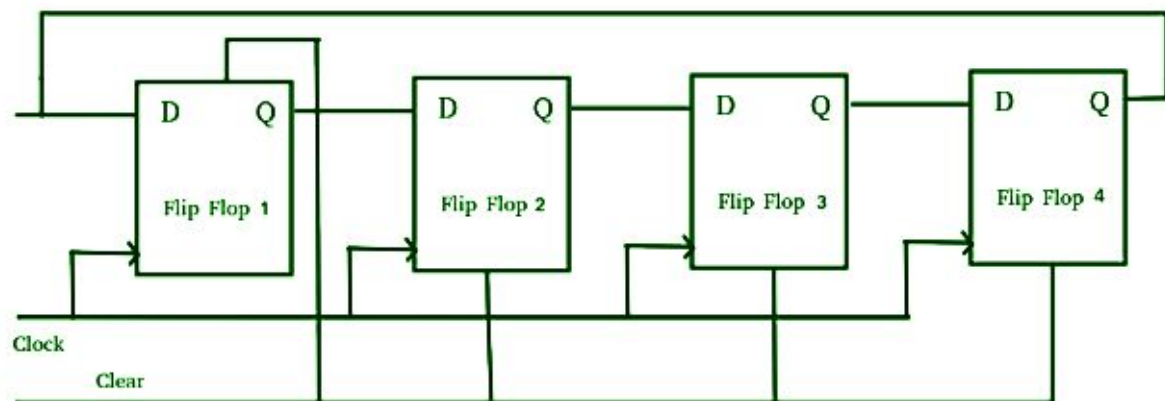
Shift Register Counter –

Shift Register Counters are the shift registers in which the outputs are connected back to the inputs in order to produce particular sequences. These are basically of two types:

1. Ring Counter –

A ring counter is basically a shift register counter in which the output of the first flip flop is connected to the next flip flop and so on and the output of the last flip flop is again fed back to the input of the first flip flop, thus the name ring counter. The data pattern within the shift register will circulate as long as clock pulses are applied.

Clock Pulse	Q1	Q2	Q3	Q4
0	1	0	0	1
1	1	1	0	0
2	0	1	1	0
3	0	0	1	1

A Ring counter is generally used because it is self-decoding. No extra decoding circuit is needed to determine what state the counter is in.

2. Johnson Counter –

A Johnson counter is basically a shift register counter in which the output of the first flip flop is connected to the next flip flop and so on and the inverted output of the last flip flop is again fed back to the input of the first flip flop. They are also known as twisted ring counters.

The logic circuit given below shows a Johnson Counter. The circuit consists of four D flip-flops which are connected.

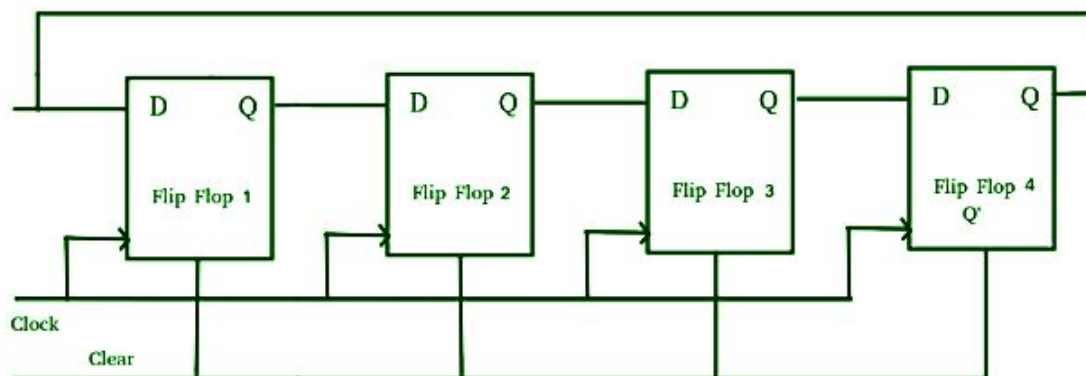
An n-stage Johnson counter yields a count sequence of $2n$ different states, thus also known as a mod- $2n$ counter.

Since the circuit consists of four flip flops the data pattern will repeat every eight clock pulses as shown in the truth table below:

Clock Pulse	Q1	Q2	Q3	Q4
0	0	0	0	1
1	0	0	0	0
2	1	0	0	0



Clock Pulse	Q1	Q2	Q3	Q4
0	0	0	0	1
1	0	0	0	0
2	1	0	0	0
3	1	1	0	0
4	1	1	1	0
5	1	1	1	1
6	0	1	1	1
7	0	0	1	1



The main advantage of Johnson counter is that it only needs n number of flip-flops compared to the ring counter to circulate a given data to generate a sequence of $2n$ states.